Performance Modeling using SystemC and TLM 2.0

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Today’s Talk

✓ Introduction to Performance Modeling (PM)
✓ SystemC and TLM 2.0
✓ TLM 2.0 Approximately Timed (AT) Models
✓ PM at T&VS
✓ Conclusion
Introduction to Performance Modeling (PM)

Execution Speed

Module

Input

Latency

Output
Introduction to Performance Modeling

- Requires Accuracy
- Implies Timing Annotation
- Delays are measured using timing points (phases)
- Delays can be based on clock cycles
  - Simulation Performance needs to be addressed
- Models focus on performance
- Functionality Verification secondary
- Performance Models used for Design / Architecture Exploration
SystemC and TLM 2.0

- **SystemC (C++ Class Library)** introduced for higher abstraction (typically no clocks)
- Implies faster simulations (~ X 1000 to X 10,000 times faster than RTL)
- **TLM 2.0** focuses on communications between modules (sockets)
  - Sockets encapsulate comms methods, DMI, Debug
  - Comms use transaction objects (Generic Payload)
- **A Large Multi-Core SoC Modeled using SystemC and TLM 2.0** can boot Linux in seconds
SystemC and TLM 2.0

- **TLM 2.0 defines two abstraction levels**
  - Loosely Timed (LT) Modeling
  - Approximately Timed (AT) Modeling
- **LT is the higher abstraction level of the two**
  - Implies focus on simulation performance
  - Large SoC modeling will employ LT
- **AT features accuracy**
  - Typically used for Performance Modeling
  - Can feature clock cycles
- **TLM 2.0 is a standard for interoperability**
TLM 2.0 AT Models

- AT Modeling introduces timing points (phases)
  - Delays between phases model performance
- Four phases defined (BEGIN_REQ, END_REQ, BEGIN_RESP, END_RESP)
- Phases can be extended. For example FIFO_AVAILABLE, FIFO_FULL etc
- Three standard communication schemes (Single Phase, Two Phase, Four Phase)
  - This can be extended
TLM 2.0 AT Models

- The communications feature three paths
  - Forward Path, Backward Path, Return Path

![Diagram showing TLM 2.0 AT Models with Module A and Module B, showing Forward Path, Backward Path, and Return Path connections.](image-url)
TLM 2.0 AT Models

- **Timing Points**
  - Return Path status indicates timing point presence
Performance Modeling @ T&VS

- **AT Modeling of SoC Sub-Systems**
  - Memory (LPDDR4)
  - Display
  - Others like Video Codec

- **Models include performance delays**
  - Configurable
  - Allow Design / Architecture Exploration

- **Models allow debug during simulation**
  - Transactions visibility including payload, phase, return path status
Performance Modeling @ T&VS

- Simplified View

- Stimulus
- Performance Model
- Monitor

Control

Delay Configuration (DMI)

Debug Interface
Performance Modeling @ T&VS

- **Memory Mapped Design**
  - Leverage TLM 2.0 Generic Payload (GP)
  - AXI4 mapped to GP with extended phases

- **Sub-Block Logic Design**
  - Ports and Exports

- **Clock**
  - Emphasis on Simulation Speed
  - Design not sensitive for computation
  - Delay Representation
  - Update Output
Conclusion

- Performance Modeling
  - Design Exploration
  - Performance Verification
  - AT Modeling Style
  - Focus on the delays rather than accurate functionality
Conclusion

Thanks!