Digital to Mixed-Signal Verification of Power Management SOCs Using Questa-ADMS

M. Behaghel
A global leader in wireless technologies

Leading supplier of platforms and semiconductors for wireless devices

Fabless company supported by extensive semiconductor manufacturing experience and telecom heritage

Truly global with a workforce of more than 85% of employees in R&D
Investing to win

- True multimode RF
- Architecture & System level power design

- Partnership with STMicroelectronics
- Latest ARM cores
- Optimized process technologies
- Aggressive nodes

- 40nm Combos
- Integrated
- Interoperability

- Multi-core architectures
- Low power consumption

- Power management and RF

- 3D Graphics, HD video, audio, imaging

- 2G, EDGE, WCDMA, TD-SCDMA, HSPA, HSPA+, LTE

- GPS, Bluetooth, HDMI, Wi-Fi, USB, FM

- Open OS, Frameworks

- Leading GPU
- Power-optimized multimedia
- Lowest power audio

A complete portfolio with multimode modems, flexible and scalable solutions

Complete platforms
Outline

- AMS/RF Verification: what is the best tradeoff
- Modeling
- Netlisting Tips: How to fit analog specificities in a digital mold
- Verification of the electrical behavior
- Results
AMS/RF Verification

What methodology should we choose?
AMS/RF design simulation needs
Complexity of AMS/RF verification

- Verification of Top Digital SOCs:
  - Proven methods/techniques to check integration, functionality,…
  - Done in specific verification teams
- For AMS/RF, designs are smaller but there are extra needs
  - Who does the verification? Do they have analog or digital background?
    - Analog and digital worlds are very different. How do they understand each others needs, language?
  - Who does the top level assembly (analog design based on a schematic)
    - Need to generate a netlist derived from this schematic
    - Netlister needs to take into account analog/digital blocks
  - How do I simulate the digital with the analog parts?
    - How can I make the best trade off between speed and accuracy?
  - Electrical functionality: how will the design behave electrically?
    - Interaction of blocks together
    - External Loads
  - How should results be managed?
    - Digital : simulation times very short. Can be rerun if questions
    - Analog/mixed : long simulation times + multiple configurations for the same stimulus
  - Other questions:
    - Will there be a verification of the IC at platform level?…
- **The Verification methodology should be the best tradeoff for all of these questions.**
Example of a functionality in an AMS power management design

- **Supply1**
- **Reference**
- **TempSensor**
- **ADC**
- **Digital**
- **Supply2**
- **cell1**
What do we want to check in a design?

### Type of errors

<table>
<thead>
<tr>
<th>Error Type</th>
<th>Description</th>
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<td>IP performance, characterization</td>
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</table>
Simulation flows available today

- Analog SPICE
- Fast SPICE Co-simulations
- Mixed AoT Simulations (VHDL-AMS)
- Mixed DoT Simulations
- Full Digital
# Flow Coverage

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Modeling
Modeling: Why do we need models?

- To simulate analog behavior with digital blocks
- To speed up simulations (clocked blocks)
- To do verification in top down approach:
  - not all of the functionality is implemented yet
- Check states that IPs are not intended for:
  - Connectivity
  - Power Domain
  - Biasing
Modeling: What is in a model?

- Checks
  - Power supplies/Grounds
  - Biasing (N/P) + value
  - Clock frequency
  - Connection checks

- Basic functionality
  - For top simulations, the functionality should be a compromise between speed and accuracy.

- Example:

```plaintext
s_target <= (VPOS - GND) + (VDIG_NN - GND);

VOUT <= VPOS WHEN to_X01(BYPASS)='1'
  ELSE 0.0 AFTER g_tfall WHEN s_enable_global=FALSE
  ELSE 0.0 AFTER g_tfall WHEN to_X01(EN)=0'
  ELSE s_target AFTER g_trise;
```
Modeling: Behavior should be a compromise between speed and accuracy
Our choice: Use VHDL-RN models to represent the analog behaviour
VHDLRN Modeling Methodology: VHDL+Real numbers package

- Digital pins: type STD_LOGIC
  - Can be plugged directly to digital blocks
  - Directions: IN, OUT, INOUT

- ANALOG pins: custom resolved type RREAL
  - Currents and voltages are treated in the same manner
    - 10.0e-6 for currents and 1.2 for voltage for example.
    - Currents: + if going to a ground / - if going to a supply
  - User-defined high impedance value: -10.0
  - Initial values: -10.0

- Netlist: VHDL-RN

Simulations are very fast

No electrical effects. Requires more electrical (fast spice/mixed) simulations

All analog cell need to be modeled
Resolution function

- Resolution if value inferior to 1.0e-3 (Current): SUM
- Resolution if value superior to 1.0e-3 (Voltage): AVERAGE
- High Impedence not taken into account: -10.0 ignored
- Possibility to have non controlled inouts
Netlisting Tips

How to fit analog specificities in a digital mold
Netlisting: Analog specificities

- Our designs are analog on top. We need to generate a netlist of the design
- Several problems:
  - How can we deal with analog instances that are left on top?
  - How can we connect types RREAL to STD_LOGIC?
  - How can we deal with INOUTs
  - How can we deal with pullup/pulldown, 1 wire communications…
  - How to check supplies on a digital block?
Netlisting: Analog devices

- In VHDL-RN methodology, all components must have a model
  - Capacitors and Diodes can be removed from the netlist
  - A resistor can be shorted
  - A resistor bridge must be modeled
Netlisting: Type conversion functions

- Conversion functions are defined in the package \((\text{real2stdlogic} \text{ and } \text{stdlogic2real})\)

- They will be inserted automatically by the netlistser

```vhdl
MYINST : MYCELL
Port map(
    PORT1 => NET1,
    PORT2 => real2stdlogic(Net2)
);
```
## All items not covered by digital verification

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Verification of Electrical Behavior
Mixed simulation for Macrocells Needs

- Complement the Digital on top simulations with mixed simulations
  - Top simulations are based on models: they do not cover analog effects
  - Need: Simulate the spice behavior of the macrocell in the top environment.
    - Power-up, power-down: supply stability
    - Interfaces with other blocks: control currents and voltages, rising time, gain, settling time
    - Behavior of the block with a top stimuli

- Simulation characteristics:
  - Transient simulations
  - Some simulations can have loops between analog and digital
Questa ADMS Platform

DAC 2012 - Questa ADMS Suite Session
From digital to mixed simulations

1. Run and optimize the pure digital simulation inside Questa ADMS as a sanity check

2. Create the mixed configuration
   - Converters
   - Simulation characteristics
   - Simulator command file
   - Spice netlists for blocs to be simulated in analog

3. Run the mixed simulation
Example of a mixed functionality

![Diagram of mixed functionality](image-url)
Automatic converter insertion

- Converters are inserted automatically between 2 types:

<table>
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<th>Digital $\rightarrow$ Electrical</th>
<th>Electrical $\rightarrow$ Digital</th>
</tr>
</thead>
<tbody>
<tr>
<td>STD_LOGIC</td>
<td>D2A_VOLTAGE_STD_LOGIC VHI=1.8; VLO=0.0</td>
<td>A2D_VOLTAGE_STD_LOGIC VTH1=0.6; VTH2=1.2</td>
</tr>
<tr>
<td>RREAL</td>
<td>D2A_VOLTAGE_REAL D2A_CURRENT_REAL</td>
<td>A2D_VOLTAGE_REAL A2D_CURRENT_REAL</td>
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- But the default value may not always be correct:
  - VOLTAGE/CURRENT converters
  - Parameters: It may be necessary to change the supply value for digital signals:
    - D2A_VOLTAGE_STD_LOGIC: ‘1’ $\rightarrow$ VLO=0.0, VHI=1.2
Converters for electrical $\rightarrow$ VHDLRN conversion

**Diagram: ELECTRICAL $\rightarrow$ REAL**

- **T_IN**
  - $V_{T\_IN}$
  - 1.2
  - $\Delta_Y$
  - 0.0
  - $1.2-\Delta_Y$
  - 0.0

- **S_OUT**
  - $S\_OUT\.value$
  - $\Delta_X$

**Flow:**
- SPICE $\rightarrow$ ELECTRICAL $\rightarrow$ REAL $\rightarrow$ DIGITAL
Results

Testcases run on a power management SoC
Case 1: IC startup

- Instances generating the mandatory startup powers and controls are simulated in analog description: SUPPLY1 regulator, REFERENCE, MONITORING, etc...

- Analog content: 12k devices, 5k nodes
Case 1: IC startup - Configuration setup

**Table:**

<table>
<thead>
<tr>
<th>NAME</th>
<th>DIR</th>
<th>TYPE</th>
<th>CONVERTER</th>
<th>SOURCE</th>
<th>PARAMETERS</th>
</tr>
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<tbody>
<tr>
<td>GNDAVSS</td>
<td>IN</td>
<td>real</td>
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**Diagram:**

[Diagram showing instance and cell configurations]
Case 1: IC Startup - Results

- Fast simulation in top level context
  - > sanity checks that can be run often
  - > enhances confidence in top level behavior

- CPU time: 15min Questa ADMS Premier 4CPU

- Allows to track bugs that could be missed otherwise
  - > found 4 diodes inserted in reverse on the main reference voltage (on the encapsulation of the IP, so standalone IP simulation could not see it)
  - > critical bug highly impacting startup behavior detected during simulation
Case 2: Macrocell validation: GPADC

- Same configuration as default startup + all instances generating power for the GPADC are in spice (VPLUS2, REFERENCE2) + the GPADC

- Validation of the analog behavior with its digital connections
  - controls coming from the main digital core
  - feedback sent to the main digital core
  - validation of the IP encapsulation (level-shifters, analog feedbacks, …)

- Analog content: 22k devices, 11k nodes
Case 2: Macrocell validation: GPADC: Results

- CPU time: 3h15 Questa ADMS Premier 8CPU

- Allows to track bugs that could be missed otherwise
  - found a misalignment in between the digital core and the IP around the DATAREADY behavior, which caused that the GPADC had 50% of failure on conversion requests!
  - impossible to detect during standalone IP simulation as the controls are generated by the designer
  - very unlikely to detect during model vs schematic simulation as well, as controls are usually reused from the standalone IP simulation
  - a critical bug highly impacting the GPADC main behavior detected during simulation
Conclusion: Interest of Digital on Top mixed flow

- Full digital simulations very fast for connectivity and functionality verifications
  - Accuracy depends on model accuracy
- Stimuli is the same as a full digital stimuli:
  - Simulation can be prepared and optimized in digital
  - The same regression procedures can be used
- Possible to switch spice blocks very low in the hierarchy
- Possible to use spice or fast spice simulators
- Simulations can be done early (does not need spice netlist for all blocks)

- A good solution to see details in a design with the accuracy of a spice simulator
# Conclusion: choose the best solution for each problem

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<td>IP performance, caracterisation</td>
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<td></td>
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<td>★★★★</td>
<td></td>
</tr>
</tbody>
</table>
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