Analyze system performance using IWB

Interconnect Workbench
Dave Huang
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Information

- Personal Speech of personal experience
- I am on behalf on myself
Interconnects Are at the Heart of Modern SoCs

Verification Challenges:

- Checking system behavior
  - Point to point data integrity
  - Verify system behavior

- Understanding system scenarios
  - Manage data flow from multiple protocols
  - Concurrent scenarios

- Cover all system scenarios

- Validate system performance
Analyzing Performance: Influence

Focus for performance of a path requires us to consider other masters that may influence the delay.

Hardware influences:
- Thin links, NIC-400 configuration, QoS, L2 Cache Speed, DDR Controller speed.

Scenario influences:
- Local traffic conflict, ACE-Lite Traffic, Processor Activity
- Modeling all these HW artifacts in TLM is impractical. Accurate performance analysis must therefore use cycle-accurate RTL models.
Cadence® Interconnect Workbench
Pre-integration Cycle-accurate Performance Analysis and Verification

System IP Data
- CoreLink 400 System IP RTL & IP-XACT
- IP-specific Traffic Profiles
- Cadence VIP Library for AMBA®

Interconnect Workbench Assembly
- UVM Testbench
  - Manual SoC Testbench
  - SoC Traffic Testbench

Interconnect Workbench Analysis & Debug
- Incisive
  - Performance Measurements
  - Performance Analysis
  - Tune Architecture

Performance GUI

Benefits
- Shorten performance tuning and analysis iteration loop from days to hours
- Reduce testbench development time from weeks to hours

For Interconnect IP Integration
- Performance of use case traffic loads
- Verify configuration functionality

For SoC Integration
- Validate performance in context of IPs
Cadence® Interconnect Workbench
Automated Testbench Assembly for CoreLink 400 System IP

Architectural Information
AMBA® Designer
User Configuration

CoreLink 400 System IP RTL & IP-XACT
Cadence AMBA VIP Library

Interconnect Workbench Assembly

UVM Testbench
Testsuite
vPlan
SimVision config
Scripts
IWB Generate Operation **(Verification) Testbench**

Starting IWB:
IWB: (c) Copyright 2012 Cadence...

#### IWB CONFIGURATION ####
- library path set to project_libraries
- library name set to iva_nic400_mp5x8
- XML file path set to <...>/nic400_mp5x8.xml
- target path set to fabric_target
- package prefix set to iva
- platform configured to UVM_E SIM

#### STARTING GENERATION FLOW ####
- IMPORTING THE DUT
- BUILDING THE HDL TESTBENCH
- BUILDING THE UVM TESTBENCH

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**<prefix>_nic400_mp5x8_(env|tb)**

- **Test Suite**
- **Virtual Sequencer**
- **Routing Model**

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![Diagram](image.png)

- PASSIVE Agent
- ACTIVE Agent
- RTL-shell
- AXI4™ Master/Slave Interface
- AXI3 Master/Slave Interface
- AHB-Lite Master/Slave Interface
- APB Master/Slave Interface
IWB Generate Operation (Performance Testbench)

Starting IWB:
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######## STARTING GENERATION FLOW ########
IMPORTING THE DUT

BUILDING THE HDL TESTBENCH
BUILDING THE UVM TESTBENCH
GENERATING VERIFICATION CONTENT

GENERATION FLOW COMPLETE

Verification Content
UVM e/SV Testbench
VIP Configuration
vPlan
(Perf) Test Suite

PASSIVE Agent  ACTIVE Agent  RTL-shell
Performance Generator  AXI4™ Master/Slave Interface  AXI3 Master/Slave Interface
AHB-Lite Master/Slave Interface  APB Master/Slave Interface
Generate Interconnect Testbench

CoreLink AMBA Designer

Interconnect Workbench
- Testbench Generation
- VIP
- Meta-data Library

System Development Suite
- Functional Verification Platform
  - Incisive
- Verification Computing Platform
  - Palladium XP

Cascaded Interconnect
- NIC-400
- CCI-400
Generate Interconnect Testbench

CoreLink AMBA Designer

Interconnect Workbench
- Testbench Generation
- VIP
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Cascaded Interconnect
- NIC-400
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Generate Interconnect Testbench

CoreLink AMBA Designer

Interconnect Workbench

Testbench Generation

VIP Meta-data Library

IP-XACT

Generate

Cascaded Interconnect

NIC-400

CCI-400

Virtual Sequence

Routing Model

Generated Testbench

System Development Suite

Functional Verification Platform

Verification Computing Platform

Incisive

Palladium XP

Performance Metrics

Verification Metrics
Cadence® Interconnect Workbench
Automated Testbench with Normal IWB flow

Architectural Information

AMBA® Designer

User Configuration

CoreLink 400 System IP RTL & IP-XACT

Interconnect Workbench Assembly

Cadence AMBA VIP Library

UVM Testbench

Testsuite

vPlan

SimVision config

Scripts
Cadence® Interconnect Workbench
Automated Testbench with New IWB Flow

Architectural Information

Standard Format

User Configuration

Meta Data file

Interconnect Workbench Assembly

Cadence AMBA VIP Library

UVM Testbench

Testsuite

vPlan

SimVision config

Scripts

Testsuite

vPlan

SimVision config

Scripts
Why is A New Flow Needed?

- Modified AMBA buses are used to save power consumption and improve performance.

- Every customer has every specific feature on interconnect structure such as memory interleaving and (AMBA + NOC).

- IP-XACT can't handle customized buses & specific interconnect structure.
How to Create Real Transactions?

- Most of masters (Multimedia IPs) generate periodic transactions at real working
- Require specific traffic generator to create periodic transactions
- Traffic Synthesizer can mimic the real master's working
Scenarios for Performance Analysis

- Why is the user interested in the worst case scenario?
  - Define Hardware Specification

- Need the various scenarios
  - Look for optimized using modes considering DVFS and QoS
  - Search for an optimized interconnect structure. Various Scenarios help the user find some weak points of bandwidth and latency.
Worst Case Scenario Example

- MPEG4 Video (How many f/s?)
- 3D Graphics with Scaling (How many f/s?)
- Camera is working with Scaling (How many f/s?)
- How many windows are overlaid?
- On Screen Characters with Rotating
Which Master & Slave are Concerned about Performance Analysis?

- Typical Wireless ARM based SoC

- Multimedia Masters
  - GPU : 3D Graphics
  - MFC : MPEG4 Video
  - Display : Overlay Windows
  - CAMIF : Scaling, Rotating, Camera Interface

- Performance of the "Memory Funnel" is key to system performance
  - Slave : Memory Controller
# Information for Traffic Synthesizer

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How to Analyze Performance
Overview of IPA

- Shows which slave is popular
- Shows overall transaction data
Maximum Latency in the Worst Scenario

- Points the maximum latency
- Shows the detailed information
- Shows the overlapped transactions
Compare with different QoS values

- Same Master & Same Scenario

QoS value is High

QoS value is Low

Two different Runs
Checks with User Definition - Latency

- Added User's Checks
- Violation Transactions
- Each Violation Transaction
Checks with User Definition - Bandwidth

- Added User's Checks
- Violation Transactions
- Each Violation Transaction
Checking Read Latency – Hit/Miss

- Cache Hit latency
- Cache Miss Latency
- Show the detailed Information
Summary

Interconnect Workbench for SoC Interconnect Verification, Performance Analysis

• Performance Measurement and Analysis for SoC Interconnect
  – Explore performance aspects across multiple simulations, multiple scenarios
    – QoS, Outstanding Transactions, Issuing Rate, etc
  – To optimize interconnect
    – Topology, QoS Scheme, Transaction Buffer Depths, etc
  – Visualize cycle-accurate performance against a variety of scenarios
  – Assess the effect of different traffic scenarios on performance

• Automated Verification of SoC Interconnect
  – Quickly configure verification environment to the interconnect
  – Run out-of-the-box tests on the generated interconnect
  – Easily update environment to verify changes

• Mimic Real Transactions with Traffic Synthesizer
  – Easily generate periodic transactions
  – Easily implement the worst case scenario and analyze the performance