Verification Futures 2016

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Agenda

Update on Challenges presented in 2015, namely

• Scalability of the verification engines
• The rise of Use-Case Driven Verification
• SW as part of SoC Verification
Challenges today’s SoC developers face

- **Many IPs**
  - Standard I/O
    - WiFi, USB, PCI Express® (PCIe®), etc.
  - System infrastructure
    - Interconnect, interrupt control, UART, timers…
  - Differentiators
    - Custom accelerators, modem…

- **Many cores**
  - Both symmetric and asymmetric
  - Both homogeneous and heterogeneous

- **Lots of software**
  - Part of core functionality
    - Communication stack, DSP software, GPU microcode…
  - User application software infrastructure
    - Android, Linux…
Common Customer Use Models Leveraging Integrated Suite
Enables optimized verification and SW development flows
Connection Points within the suite of engines

- **Perspec™** - System-level Use-Case Verification
- **vManager™** - Plan & Management
- **Indago™, SimVision™** - Debug & Analysis
- **Verification IP**
  - **Incisive® VSP** - SystemC / Virtual Prototyping
  - **Stratus™** - High-level Synthesis
  - **JasperGold®** - Assertions, XProp, Super Linting
  - **Incisive** - Formal Verification
  - **Palladium™** - Acceleration & Emulation
  - **Protium™** - FPGA Based Prototyping
  - **Incisive-VSP Hybrid** - Low Power & Mix
  - **Indago™** - SystemC / Virtual Prototyping
  - **SimVision™** - Debug & Analysis
  - **vManager™** - Plan & Management
  - **Perspec™** - System-level Use-Case Verification
  - **Verification Acceleration with Hot Swap, Coverage Merge, UPF/CPF**

- **Common front-end with Multi Fabric Compiler**
- **Assertion Based VIP**
- **Perspec™** - System-level Use-Case Verification
Capabilities combining simulation and emulation

Common Compile
Ease of transition

Hot-swap
Balance software and hardware based execution
Time to point of interest

Coverage Merge
Faster coverage closure

Gate-level acceleration
Validate gate-level synthesis with minimal capacity overhead

Acceleration

Common Compile
Ease of transition

Hot-swap
Balance software and hardware based execution
Time to point of interest

Coverage Merge
Faster coverage closure

In-circuit acceleration
Re-use Environment
Mix abstractions
Balance by model availability

Accelerated VIP
Migrate from simulation with VIPs to acceleration with AVIPs with common library (roadmap)
Palladium Z1 Announced Q4 2015
Key characteristics
Delivering up to 5X greater emulation throughput

• Unmatched engineering productivity
  – Up to 5X greater emulation throughput
  – Up to 2.5X greater workload efficiency
  – Up to 2X faster compilation speed
  – Up to 50% higher average performance

• Scalable datacenter-class emulation system
  – IP to full SoC emulation: 4 to 576 million per rack
  – Scales up to 9.2BG with up to 2,304 parallel jobs
  – Rack-based form factor: setup in existing data center
  – Redundancy: reliability and availability

• Virtualization
  – Virtual target relocation
  – Advanced job reshaping
  – Emulation Development Kits (EDK)
  – Virtual Verification Machine (VVM)

• Best in class total cost of ownership (TCO)
  – 8X higher gate density
  – 92% smaller footprint
  – 44% better power density
  – 22 use models
JasperGold® formal verification platform

JasperGold Apps
- Formal Property Verification App
- Automatic Formal Linting App
- Design Coverage Verification App
- Sequential Equivalence Checking App
- X-Propagation Verification App
- Control/Status Register Verif. App
- Connectivity Verification App
- Coverage Unreachability App
- Clock Domain Crossing App
- Functional Safety Verification App
- Low Power Verification App
- Security Path Verification App

Visualize™ Interactive UI & Debug

JasperGold Platform Core Technologies
- Assertion Based Verification IPs for AMBA and other common protocols
- Programmable Interface via TCL
- Parallel & Multiple Engines with ProofGrid™ Manager
- Links to System Development Suite™ (Incisive, Palladium, Metric-Driven Verification, Debug…)

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Tight integration with System Development Suite

• Visualize™ features in Indago™ for simulation users

• Incisive® front-end and irun integration
• Assertion export to Incisive

• vManager™ integration
• Coverage unreachability

• Assertion-Based VIP support
• Assertion export to Palladium®
### JasperGold apps: design scope

<table>
<thead>
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<th>Scope</th>
<th>AFL</th>
<th>XPROP</th>
<th>CSR</th>
<th>FPV</th>
<th>ABVIP</th>
<th>UNR</th>
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✓ = now
✓ = near future
SoC verification needs to address:

- **Diverse Platforms**
  - Virtual Platform
  - Simulation
  - Emulation
  - FPGA Prototype
  - Silicon Board

- **Diverse Users**
  - Architect
  - HW Developer
  - SW Developer
  - Verification Engineer
  - SW Test Engineer
  - Post-silicon Validation Engineer

- **Diverse Scopes**
  - Integration
  - IP
  - Sub-System
  - OS & Drivers
  - Bare Metal SW
  - System on Chip (HW + SW)
  - Middleware (Graphics, Audio, etc.)

- **Use Case Reuse**
- **Horizontal Reuse**
- **Vertical Reuse**
- **Application Specific Components**
- **SoC interconnect fabric**
- **ARM V8 CPU Subsystem**
- **Cache coherent fabric**
- **High speed, wired interface peripherals**
  - DDR3
  - USB3.0
  - PCIe Gen 2.3
  - Ethernet
- **Low speed peripheral subsystem**
  - PMU
  - MIPI
  - JTAG
  - INTC
  - I2C
  - SPI
  - Timer

Perspec takes **use cases** defined by users.
Generates **code** that runs on embedded CPUs.
Exercising the system through **diverse relevant** scenarios.
The Solution: **Perspec™ System Verifier**

**Vertical Reuse**
- Diverse Scopes (Integration)
  - Middleware (Graphics, Audio, etc.)
  - OS & Drivers
  - Bare Metal SW
  - System on Chip (HW + SW)
  - Sub-System
  - IP

**Use Case Reuse**
- Diverse Users
  - Architect
  - HW Developer
  - SW Developer
  - Verification Engineer
  - SW Test Engineer
  - Post-silicon Validation Engineer

**Abstract Model**
- Perspec™ System Verifier
  - Reusable Use Cases
  - Naturally Model: Library provides built in content (e.g. coherence stressing)
  - Generation Automation: Tests capture user intent & use cases

**Horizontal Reuse**
- Diverse Platforms
  - Virtual Platform
  - Simulation
  - Emulation
  - FPGA Prototype
  - Silicon Board

- Multi-core Verification OS
- Many cores
- Multi-cluster Apps Processors
- 3D GPU
- DSP
- High-end
- Functional
- Real-time

- C test
- SV test
- C test
- Scripts

**Mapping to Targets**
- Delivers 10x Productivity Gain
- Generated code
New Portable Stimulus Specification (PSS) Standard
Accellera PSWG is working on developing this standard

Cadence & Mentor Contribution

Enabling industry alignment on a Portable Stimulus Specification

Contribution will help accelerate development of a standard that meets both vertical and horizontal stimulus and test reuse requirements

✓ A constraint driven model-based approach aligned with Perspec semantics and supporting graph-based descriptions of stimulus and test scenarios
✓ To learn more about the portable stimulus working group, visit accellera web site