

UCIS - The Unified Coverage Interoperability Standard

DVClub 2009

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Member UCIS TSC +

PRODUCT MARKETING MANAGER

Questa Verification Management & Coverage

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Agenda

- **The Need**
- **Who are Accellera and UCIS**
- **Progress to Date**
- **What to Expect**

Measurement Knowing When You Are Done

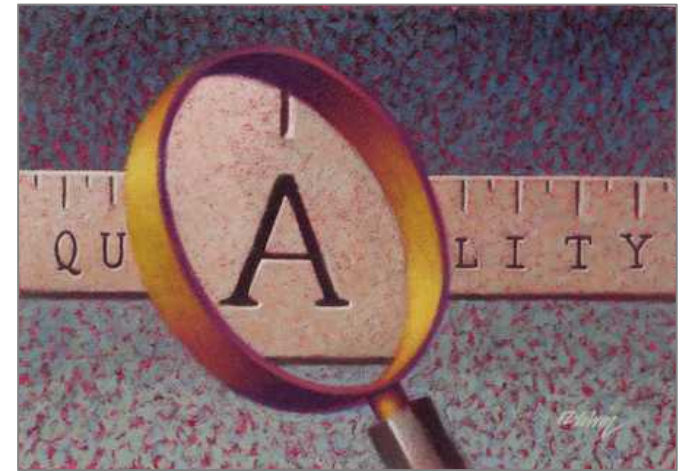
- To measure completeness requires metrics

[Lord Kelvin] .. “If you cannot measure it, you cannot improve it”

19th-century English Mathematical Physicist

- Unfortunately, there’s not a single metric that completely characterizes all aspects of a design

- Different coverage metrics represent different aspects of a design

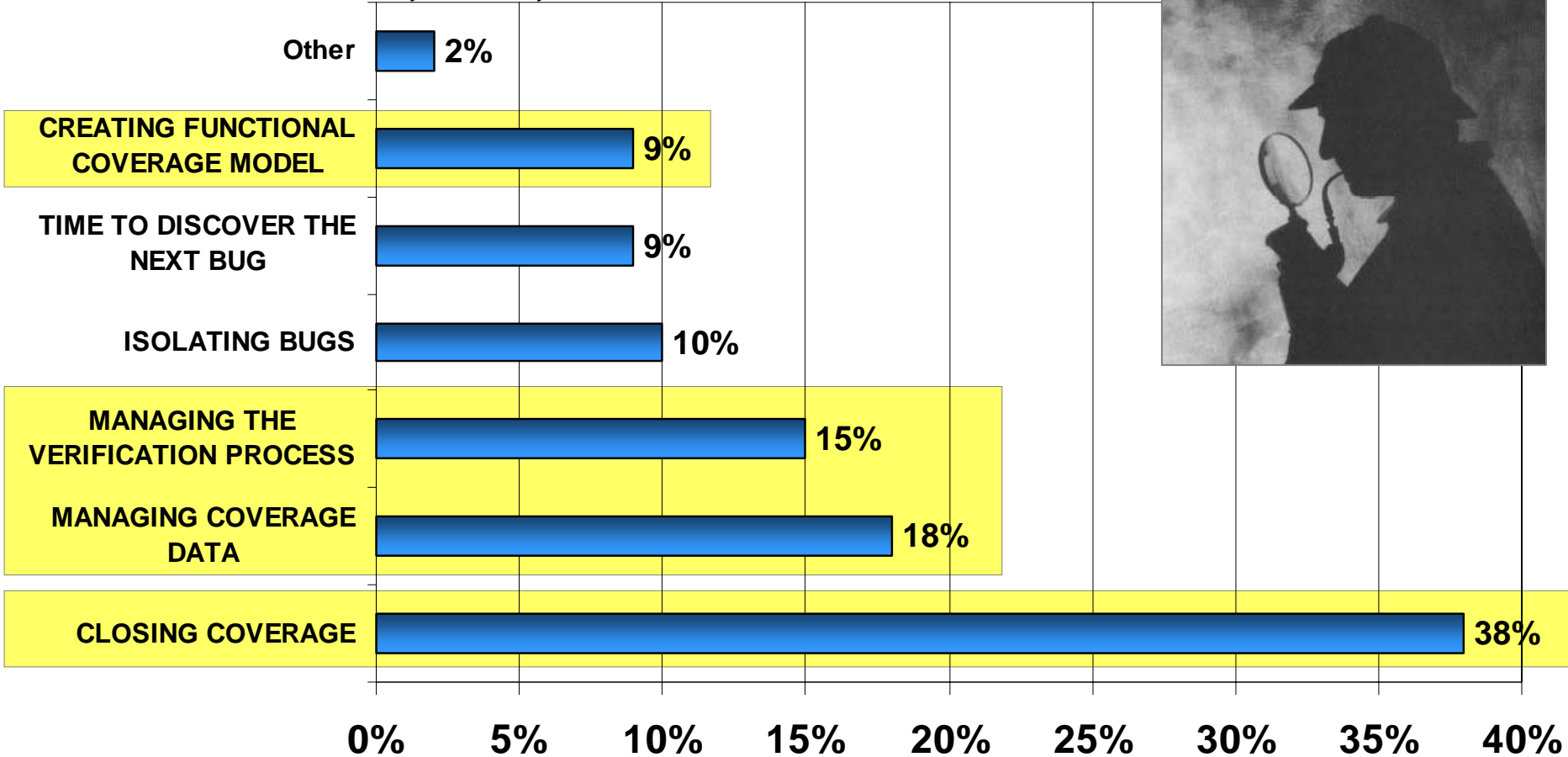


- Today’s *Total Coverage* solution requires defining, measuring, and analyzing multiple coverage metrics

Biggest Challenges Users Want Solved

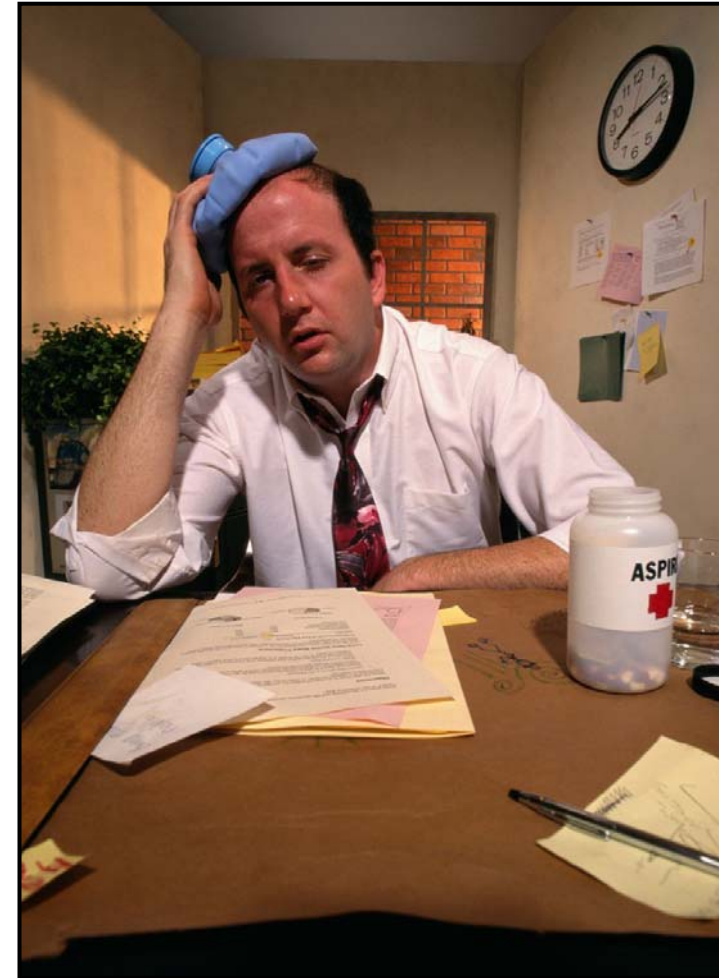
4 of the top 6 changes are related to coverage & metrics!

Study Conducted By: Far West Research



The Need For a Unified Solution

- **Verification Management**
 - Product Quality
 - Resources and Schedules
 - Costs
- **Multiple Sources**
 - Tools and Vendors
 - Metrics
 - Geographical locations, IP
- **Unification Enables Common ..**
 - Reporting and Analysis
 - Process optimization



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Who are Accellera ?



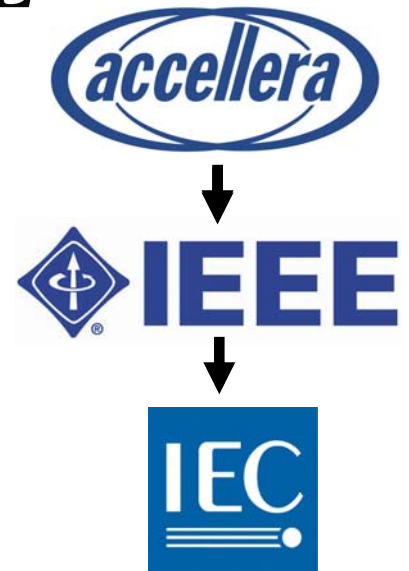
- **Formed in 2000**
 - OVI plus VHDL International
 - Industry Funded

- **Mission Statement**

To drive the worldwide development and use of standards required by systems, semiconductor and design tool companies that enhance a language-based design automation process.

Who are Accellera ?

- **Chair (Sun), Co-chair (MGC) plus Members**
 - Corporate, approve budget, TSC formation and standards
 - Associate Corporate, vote on TSC work items
 - Any non-member, monitor & inspect TSC work.
- **Policy to transfer its standards to the IEEE**
 - When the Accellera standard is solid
 - Sponsors creation of IEEE committees
 - Started with OVI, and continues today
 - Accomplishments in IEEE/IEC
 - Verilog 1995/2001, SDF, PDEF, SPEF
 - DCL, ALF, Verilog/VHDL Synthesizable Subset
 - VHDL/VITAL



UCIS Technical Sub-Committee

- Formed Nov 2006
 - Approx 130 members
 - 18 member Companies
- TSC goals are:
 - Identify interoperability opportunities
 - Define standard coverage models
 - Define an operability standard for exchange
 - Encourage user and EDA technology advancement



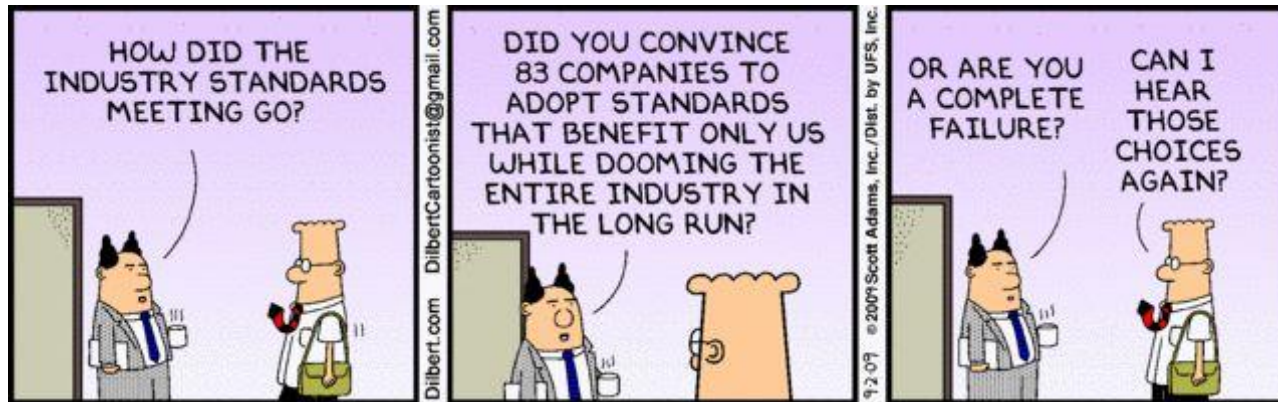
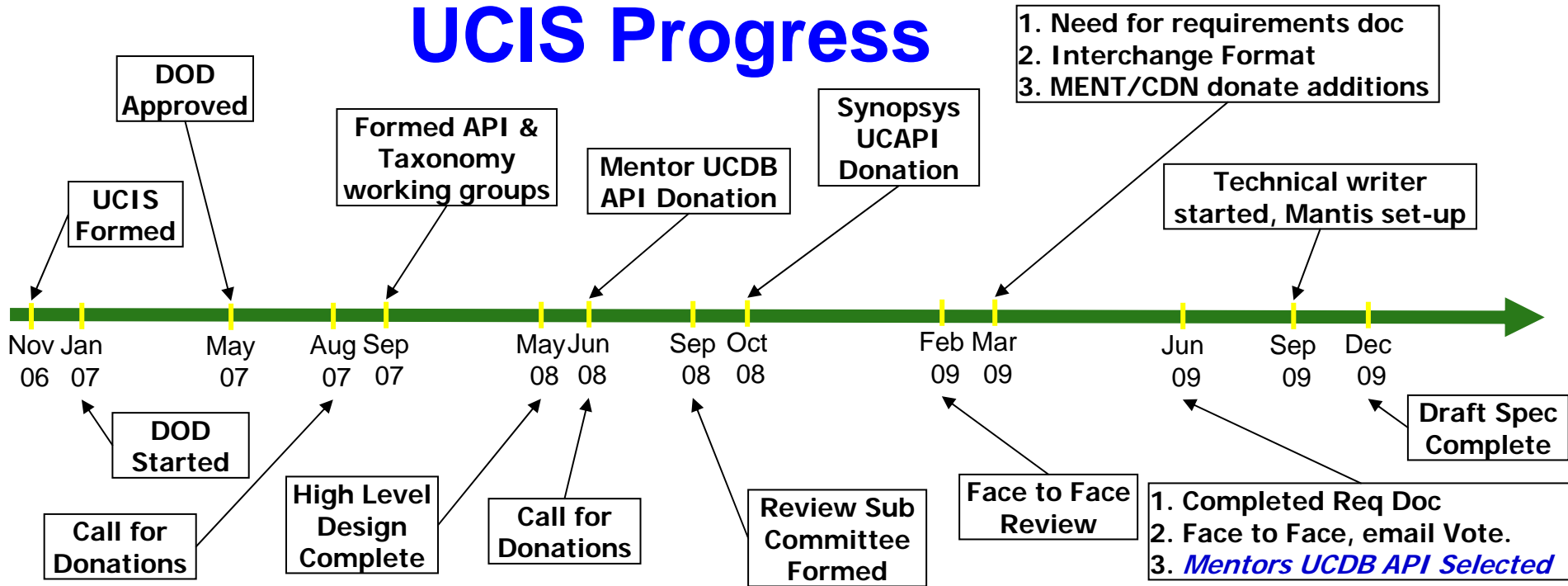
Mission Impossible



Agenda

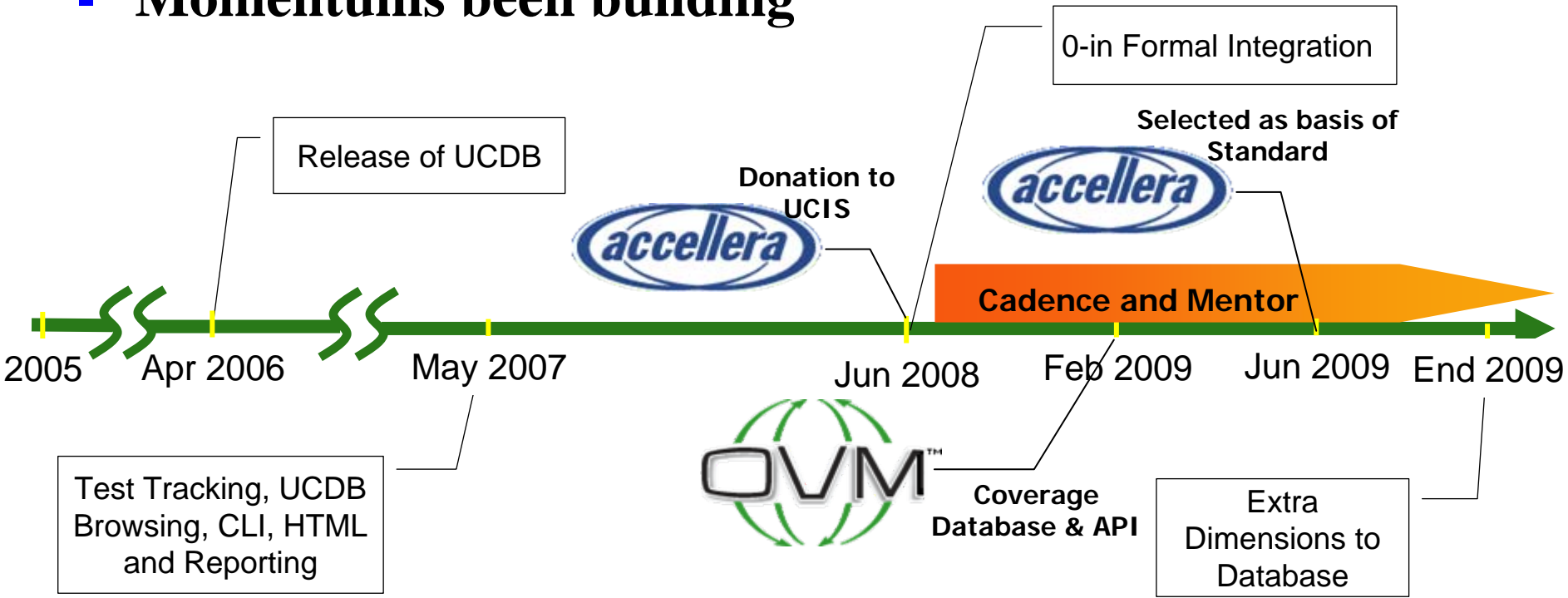
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UCIS Progress



Mentor's UCDB Development

- Developed by user requirements
- Released in ModelSim and Questa 6.2
- Continual development
- Momentums been building



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UCDB Database Overview

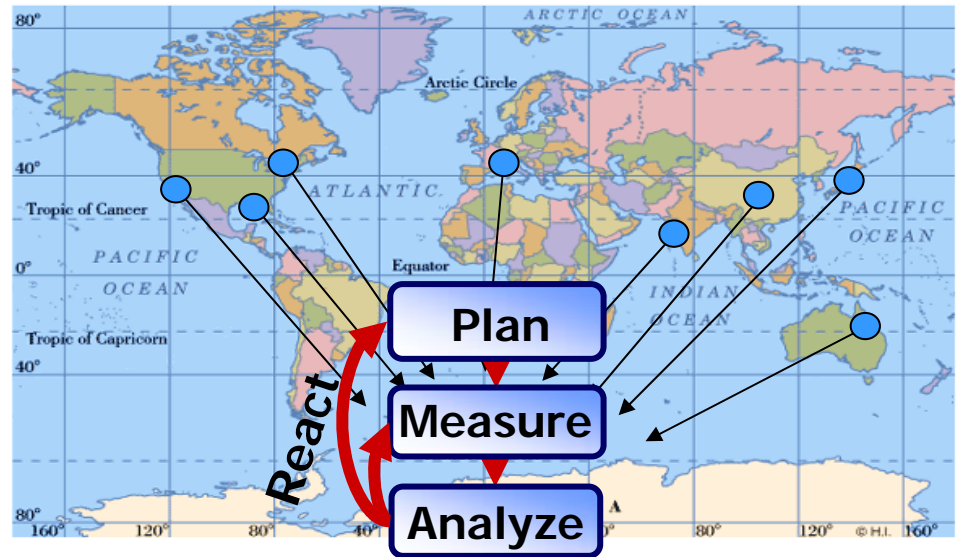
- **Proprietary Binary Format built for Verification Management**
 - SQL Performance > 3 orders of magnitude too slow
 - Built for performance and capacity
 - In memory or streaming database access
 - Used Natively by Questa and ModelSim since 2006
- **UCDB Organization**
 - One UCDB file or many UCDB files maintains flexibility
 - One for each simulation run
 - Utilities to merge/rank/report/manage
 - Three Sections of information
 - Test Record and History nodes hold information about the test/set of tests
 - Coverage data, as hierarchy of scopes related to testbench/design/test plan
 - Summary section
 - Test-associated
 - Merge maintains correlation between coverage and tests
 - Faster merging with smaller UCDB file sizes

The API

- **Low level API Routines**
 - Managing/Traversing hierarchy, coverage scopes & tests
 - Accessing, editing or creating coverage data
- **Extendable Architecture**
 - Exclude cover mechanism
 - Tagging functionality for grouping and testplan association
 - User definable attributes and coverage storage
- **Higher Level Routines**
 - Coverage calculation
 - Test association manipulation
- **Enables the Building of Application Level Functions**
 - Merging, ranking
 - Custom reporting

UCIS Will Deliver ...

- **A Data model**
 - Common coverage models
- **A Naming scheme**
 - Based on Languages
- **An API**
 - Read, Write and Edit
- **An Interchange format**
 - Import, Export



Questions ?

The image features the Mentor Graphics logo in a bold, white, sans-serif font. The word "Mentor" is positioned above "Graphics", and a registered trademark symbol (®) is located to the right of "Graphics". The background is a vibrant blue with a complex digital pattern of glowing lines, nodes, and binary code (0s and 1s).

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