# Verification Challenges


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# Where Are We Now?

- Lots of work done on IP core verification.
  - We can get this right so long as we apply enough effort.
- Chips are becoming the problem.
  - The number of cores on a chip means there are real verification challenges at the chip level.
- Verification resources are over-stretched.
  - Need to keep people focused where they really add value and automate other activities.
- Many new flows required.
  - Formal, power, ….

# The Scalability Challenge

- Core activity reuse
  - Simulations are slow even when unimportant modules are stubbed.
  - Chip-level SDF can take several days to generate.
  - Need ways to break this down and push more activities into the cores.
- System/software coverification
  - Hardware platforms are not scaling.
- Metrics and specs
  - Often use directed testing based on specs.
    - Code coverage is not suitable for chip level.
    - Functional coverage is too time-consuming and difficult to close.
  - Need better ways of validating specs and managing change.
    - For example, executable specs.

# The Verification Resource Challenge

- We spend a lot of time not doing chip verification.
  - Core issues that are only found at the chip level.
  - Troubleshooting and debugging simulation and test bench issues.
  - Time spent on multisite data management.
  - We spend time integrating diverse core environments – SV, e, SystemC, MATLAB, ….
  - Need better support for common scenarios and sources of error.
    - Issues hidden by X optimism in RTL.
    - False issues introduced by X pessimism in gates.
    - Issues introduced by incorrect timing exceptions.
    - Inaccuracies in analog models.
    - Can we find more sophisticated forms of structural coverage?
  - Need better support for cloud computing.
    - For example, GUI renders locally while compute/data intensive process is remote.
  - Need better interoperability at the chip level.

# The EDA Tool Maturity Challenge

- There are at least three languages called SystemVerilog.
  - Need everyone to implement the whole standard or agree on a subset.
- Power simulation is increasingly important.
  - Flows and formats taking a long time to mature.
- Bug reporting is increasingly difficult because of IP issues.
  - Isolating bugs is time-consuming and often requires an understanding of the bug itself.
  - Need tools to be able to extract IP-free test cases.

# Thank You!


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