The Interconnect Verification Challenge

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Test and Verification Solutions

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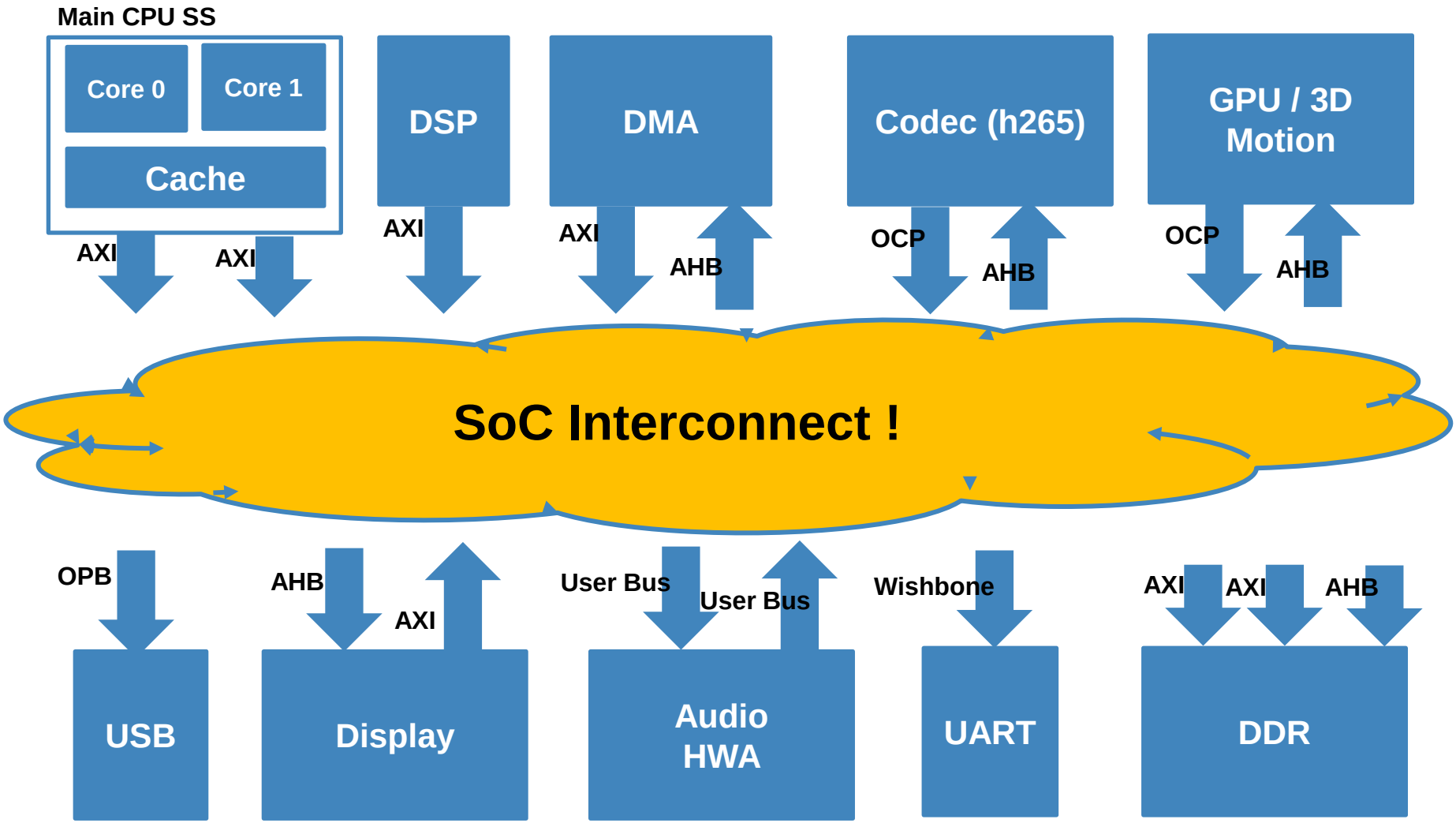
The Interconnect Verification Challenge

TVS

- What's an interconnect
- Interconnect's characteristics
- Topologies
- Transaction's Paths
- Verification Goals
- Verification Environment
- Protocol conversion
- Scoreboard features
- Scoreboard architecture

SoC Interconnect

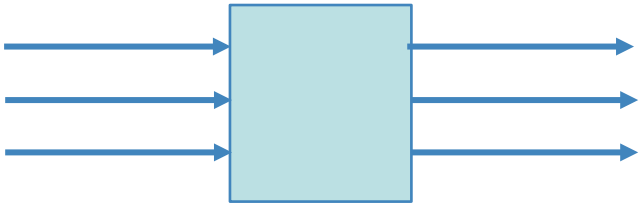


SoC Interconnect Characteristics

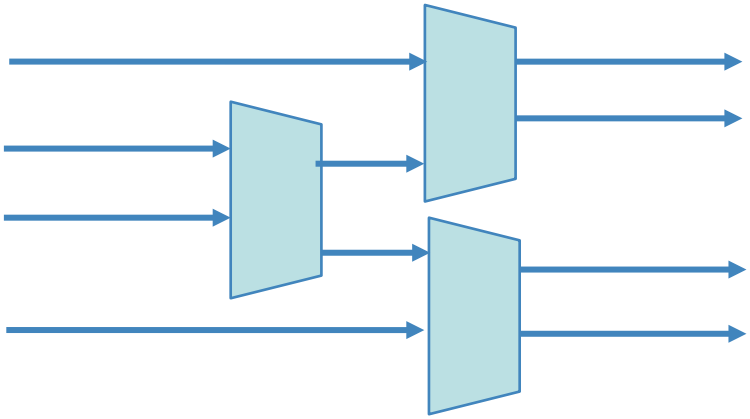
- **Master/Slave communications**
  - Protocols (AXI, AHB, APB, OCP, PLB, OPB, DCR, Wishbone, company corporate bus, …)
  - Bus Widths (16/32/64/128)
- **Memory Maps**
  - Shared memory map for all masters ?
  - Memory map clusters ?
  - One Memory map per master ?
- **Address Space**
  - Physical Address Space
  - System Virtual Memory Address Space (System MMU)
  - Virtual Address Space
- **SoC specific features**
  - Error management → invalid requests
  - Security → invalid request depending on security attributes
  - Power management
    - Invalid requests
    - Wake-Up

Interconnect Topologies

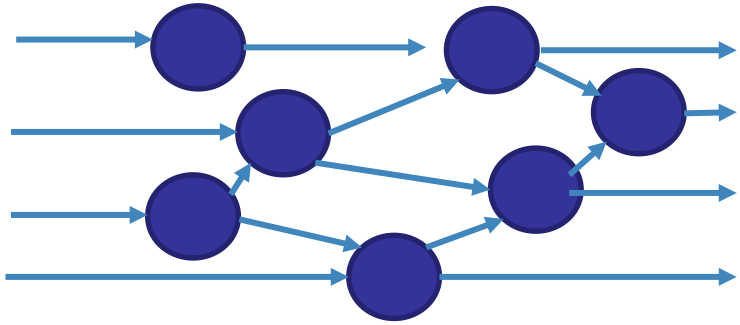
- **Shared Bus**
  - Chip select, arbiter
- **Cross Bar**



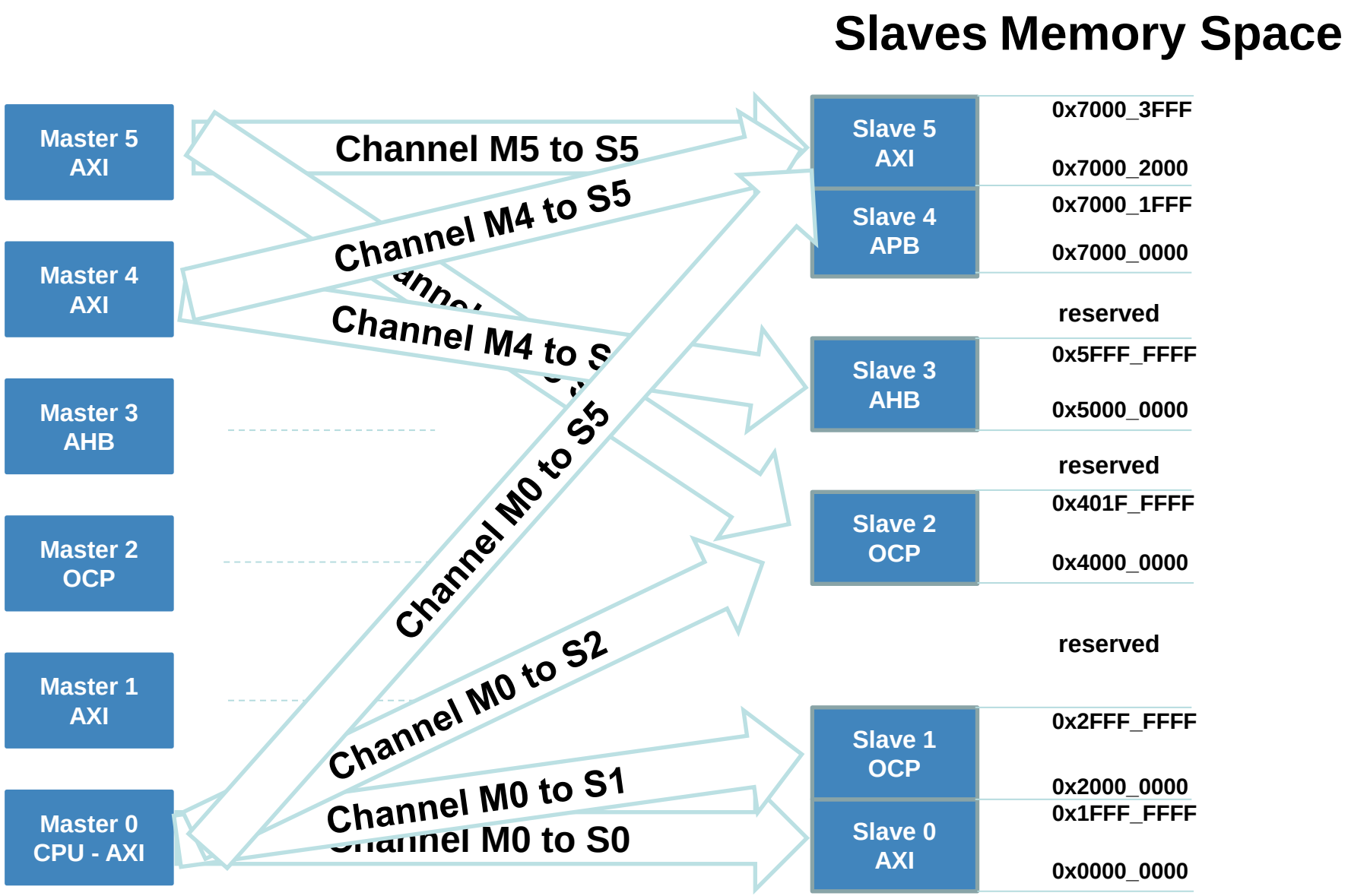
- **Muxes/Switch/Routers**



- **Network on a Chip**



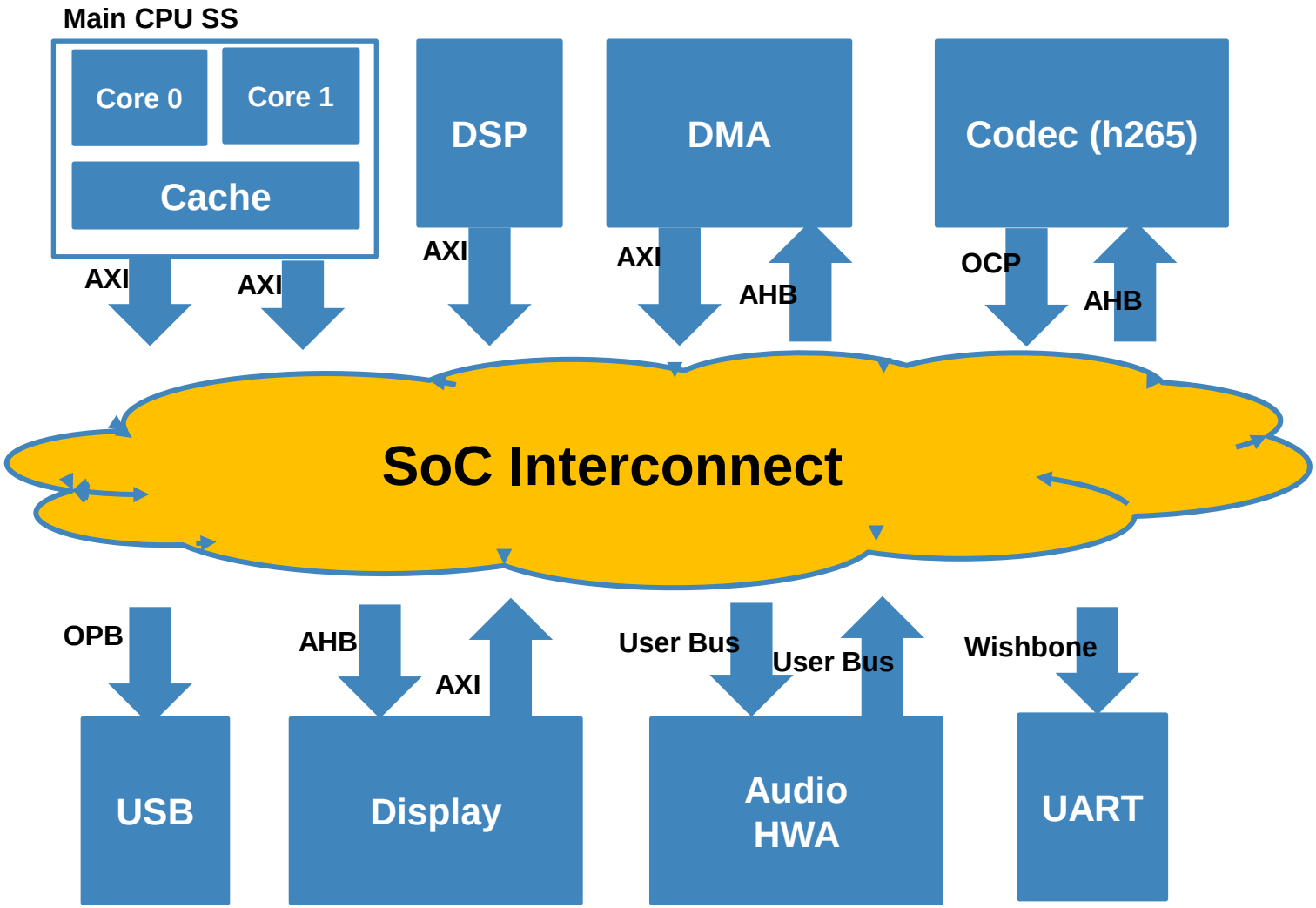
Interconnect Routes



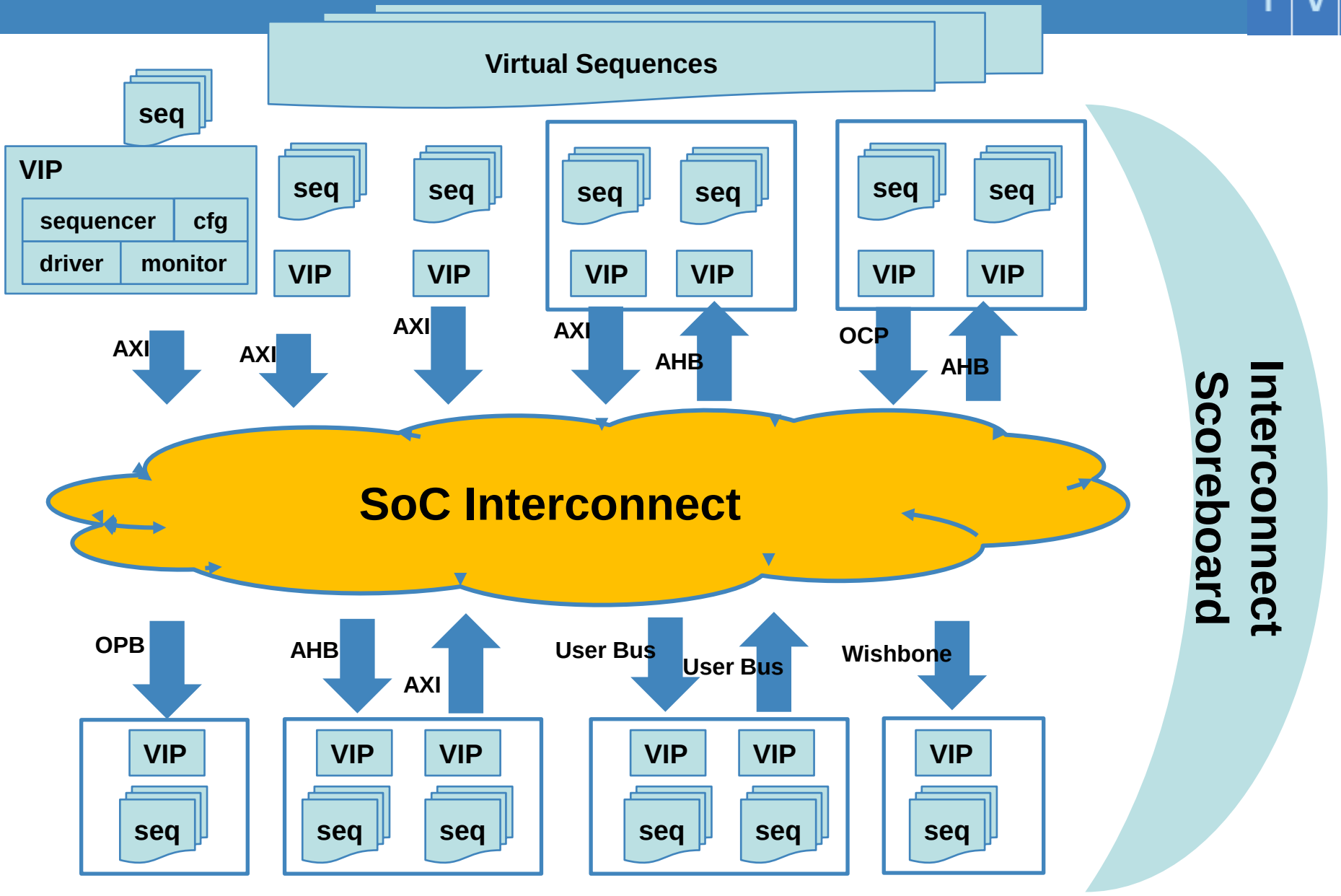
Verification Goals

- **Address Map**
  - Are all masters able to access all possible slaves ?
  - … under virtual address mode ?
  - Errors on invalid addresses
- **Protocol Sanity**
  - Are all kinds of transactions supported on each route ?
  - Are bursts/locks supported on each route ?
  - Protocol not broken under stress conditions
- **SoC features**
  - Security
    - Can secure transactions access to all slaves ?
    - Are unsecured transactions getting errors from secured slaves ?
  - Power Management Use cases
    - Are we getting error from power off slaves ?
    - Are we able to wake up a slave ?
- **Use cases**
- **Performance Analysis**
- **(Interconnect integration)**

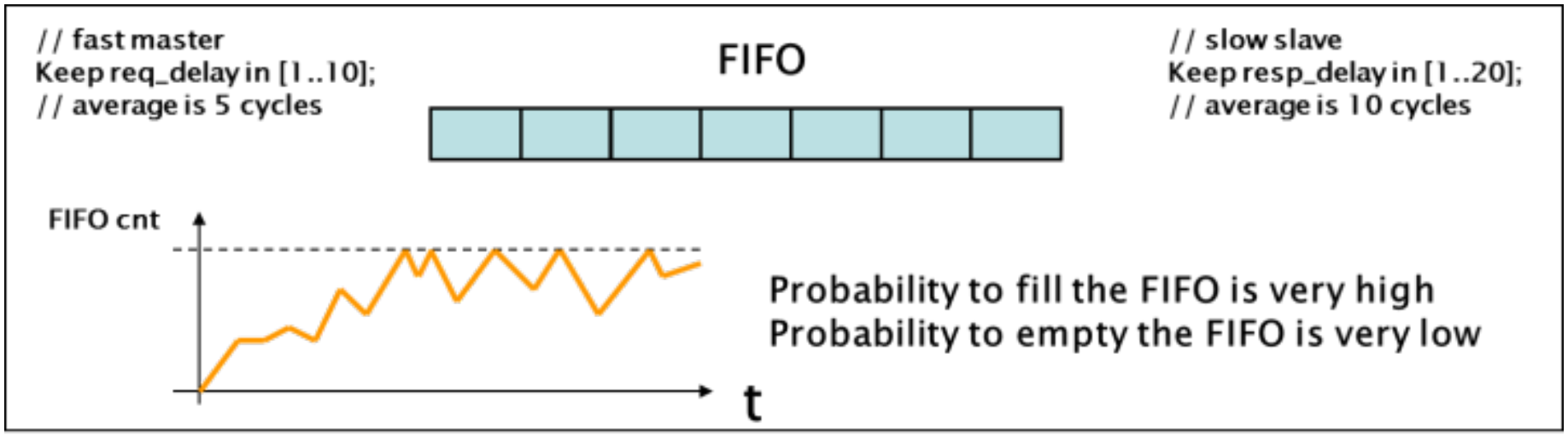
Interconnect Verification Environment

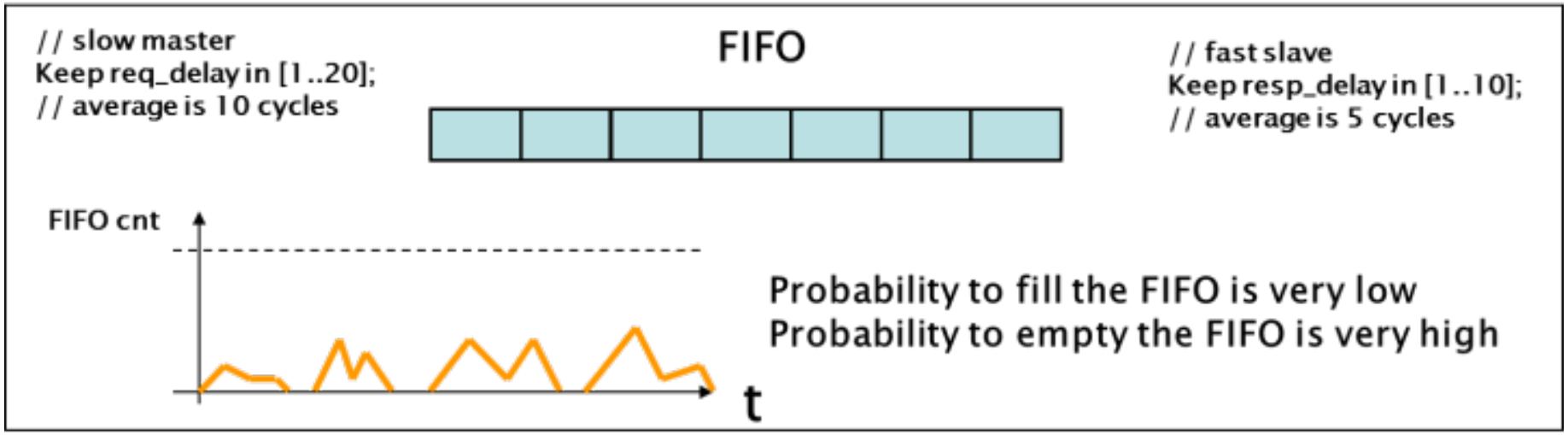


Interconnect Verification Environment



Choosing the right sequence

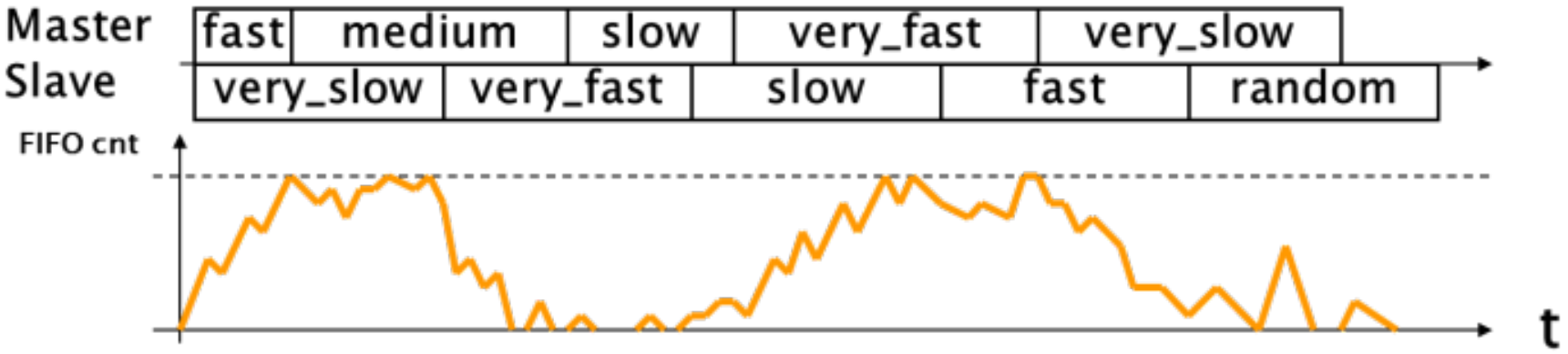




Choosing the right sequence

- **Dynamic constraints**
- **Scenarios vary over time**

➔ **Make Interconnect reaching further traffic congestions**



Protocol conversion issues

AXI transfer

Request transfer

AXI burst len=3
Size = WORD
Address = 0x3
Kind = WRAPED
LOAD

Response transfer

7	6	5	4	3	2	1	0
F	E	D	C	B	A	9	8
17	16	15	14	13	12	11	10

Converted transfers

Request transfer

LD16
Addr = 0

Request transfer

LD8
Addr = 0x10

Response transfer

7	6	5	4	3	2	1	0
F	E	D	C	B	A	9	8

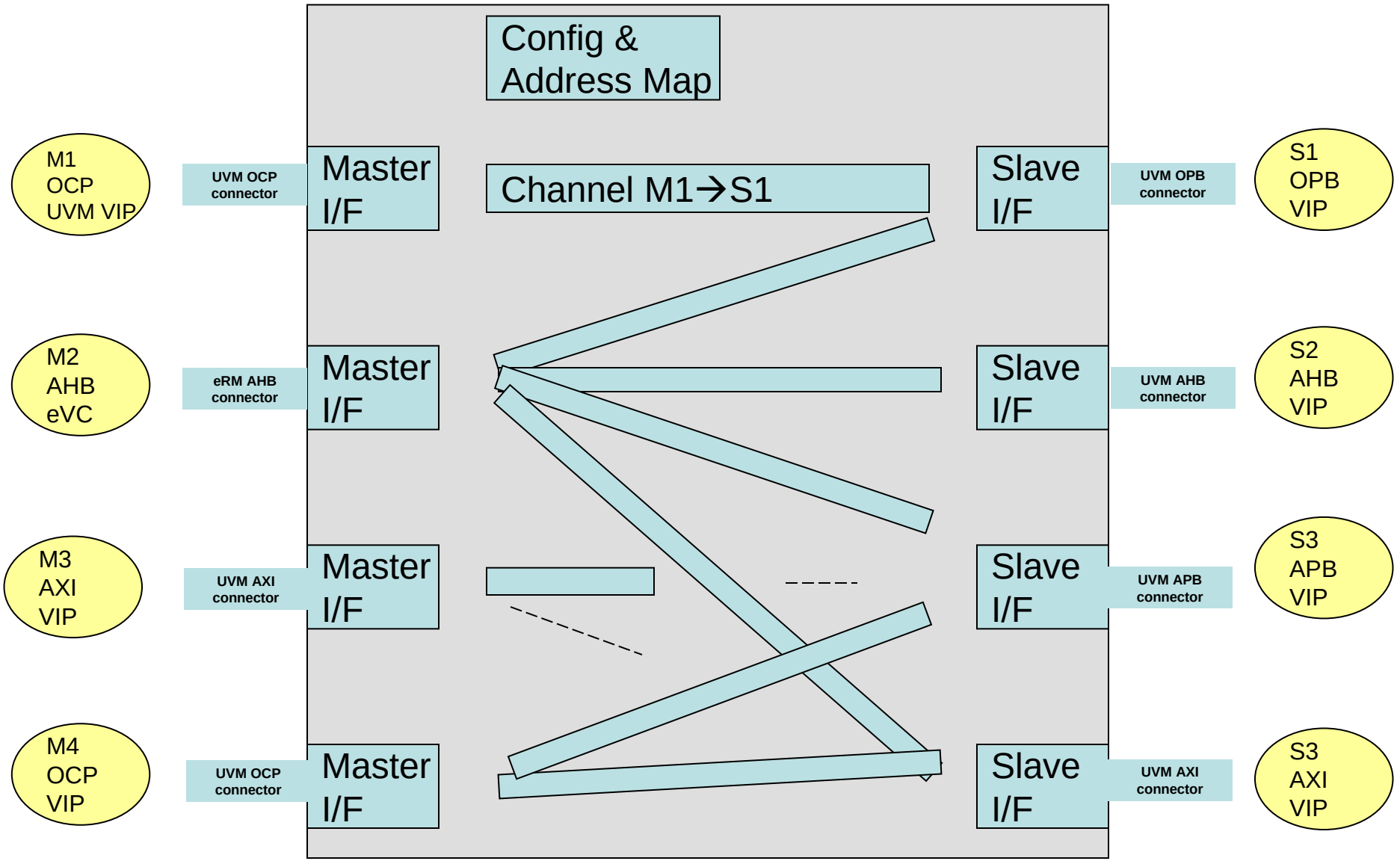
Response transfer

17	16	15	14	13	12	11	10

Scoreboard Requirements

- **Connect to any bus protocol VIP**
- **End to End transaction checking**
  - Data, direction, attributes, response, atomicity
- **Support for:**
  - Multiple address maps, Virtual address space
  - Address map reconfiguration, MMU
  - Security, Power management
  - User defined security/filtering (DRM, …)
- **Comparison policies**
  - Strict:
    - one to one transaction comparison
  - Permissive:
    - Allow transaction address realignment, dummy reads, nops
  - Per checker configuration
    - User switch on/off each checker (per path)

Scoreboard Architecture



User's experience

- **3 derivatives of a SoC Interconnect**
  - 40 masters, 60 slaves with over 200 paths
  - 5 protocols, 3 different bus sizes
  - Security Management
  - Power Management features
  - Dynamic address translations
- **Scoreboard Developments**
  - Right architecture choice is key
  - Generic features / Generic Adapters
  - Search and comparison algorithms
- **Verification results**
  - Address map specification
  - Wrong protocol translations of AXI FIXED from 64 to 32 bit buses
  - Deadlock in some traffic congestions involving bursts
  - Deadlock in power management

Conclusion

- **SoC Interconnect needs to be verified from end to end**
- **Verification Environment should address**
  - Complex scenarios
  - Stress/congestion conditions
- **Interconnect SoC scoreboard should be generic & highly configurable**
- **Scoreboard can also provide:**
  - Functional coverage metrics
  - Performance information