Shortage of Verification Resources in the Semiconductor industry

An Anonymous post on the Verification Guild commented “Without first-rate verification engineers, most of the industry will be shipping second-rate designs. Where's the glory in that?” This nicely summarizes the semiconductor industry’s need for skilled hardware verification engineers.

Over the years, design complexity and size have stubbornly obeyed the growth curve predicted by Gordon Moore. The industry is migrating towards leading edge nodes, which can hold more than 100 Million gates. The chip makers want to pack as many functions possible in their SoCs and provide as many feature additions to gain market share. And, of course, all of those features need to be verified.

A Gartner study suggests that the key industry trends in the Global Chip Design market are: Escalating cost of chip design, increasing design complexity and shorter time for new product launch. The worst thing that could happen to a Chipset company is a respin due to a buggy product. This calls for greater concerted effort to verify the complex designs and a particular need of skilled and smart verification resources to help thwart increasing development costs.

In his blog, Harry Foster of Mentor Graphics discusses the study conducted by Wilson Research Group commissioned by Mentor Graphics in 2010 on the Functional Verification trends. He feels there is a strong need to manage productivity to meet the challenging timelines. The study suggests that in 2010 over 56% of total time spent on projects was on verification. With reference to the number of engineers in the last 3-4 years, a 4% increase in design engineers has required an alarming 58% increase in verification engineers. This means that there are a lot of verification job positions open worldwide that are required to be filled.

The reasons for shortage in hardware verification resources are multifold. If we analyse why then we see that part of the problem lies with lack of structured course work and research offered by academic institutions. There is anecdotal evidence that this is being addressed. For example, in the UK Bristol University offers a Design Verification module and the EPSRC plans to significantly grow the UK funding for research into verification. However, a large scale adoption is required to fill the world-wide demand for skilled verification engineers and ensure a smooth transition for an individual from academia to industry. There is also a need for greater collaboration between industry and educational institutions to ensure students get a better perspective on the industrial verification methodologies.

There is a perception in the industry that design is more challenging than verification and thus attracts a higher salary. This is one of the reasons that junior-level engineers and university graduates prefer design over verification. We may attribute this mindset due to the lack of awareness of the challenges involved in verifying complex SoCs. But the fact is design verification requires strong analytical skills and creative thinking. There are numerous scenarios to think through not only at system/chip level but also at the application level, where things could really go wrong. With all this effort the verification team is helping their company save millions of dollars. Hence there is a greater challenge in making the design work than just designing itself.

The EDA industry has championed the case for verification where more and more automated tools were developed for verification planning and execution, which has now made it more attractive for engineers to take up verification. TVS has played its part by offering a state of the art verification management tool

(asureSign™) that helps not only to efficiently track the entire verification effort but also smart reporting of requirement status.

Design IP has enabled the design community to rise to the challenge of improved design productivity. In verification there has been the emergence of Verification IPs that provide distinct benefits in helping companies tackle the shortage of verification resources. VIPs are ready-to-integrate blocks that improve reusability and assure compliance with standard specifications. TVS with its asureVIP™ portfolio ensures semiconductor companies have less turnaround time integrating TVS VIPs into their SOC Verification environment.

Due to tight operating costs, the majority of semiconductor companies manage design teams in-house whereas for verification they rely on external service providers to fill this critical requirement. Semiconductor companies face a major challenge in locating the right skilled engineers who would minimize the transition phase and readily fit into the scheme of things. The verification engineer is required to be equipped with knowledge of protocols and standard interfaces, HVLs and latest verification techniques. The EDA companies and Doulos now provide training programs on languages and verification methodologies. TVS through its asureTrain™ goes a step beyond in offering advanced verification training programs that target project leads and program managers and helps them gain a deeper understanding of advanced verification techniques, understand the advantages and costs of those techniques and finally, develop an effective verification strategy using those techniques.

So, in conclusion, verification is currently the largest challenge facing the semiconductor industry in keeping pace with both the customer demand for features and our technical ability to add millions of gates to our chips. To see off that challenge the industry needs to continue the advances it is making in productivity, to attract graduates into verification and to ensure that those graduates have the right skills.

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TVS provides services and products to organisations developing complex products in the micro-electronics and embedded systems industries. Such organisations use TVS to verify their hardware and software products, employ industry best practice and manage peaks in development and testing programmes. TVS hardware verification services include onsite/offshore verification support and training in advanced verification methodologies. TVS also offers Verification IPs and its own Verification (EDA) signoff tool (asureSign™). TVS embedded software testing services includes methodology development, software test training and execution support services.

Note to Editors:
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Media Contact:
Mike Bartley
+44(0)7796 307958
mailto:mike@testandverification.com