Functional Verification of Today’s and Tomorrow’s SoCs

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UVM: Next Step in Standardization

• Standard language
• Standard verification language
• Standard methodology
Origin of the Species

25 years

Origin of the Species

- eRM
- uRM
- AVM
- OVM
- UVM
- TLM 1.0
- TLM 2.0
- VMM 1.0
- VMM 1.2
- RVM

Timeline:
- 2002
- 2004
- 2006
- 2008
- 2010

8 years
Increasing Complexity

Increasing Design Complexity

Advanced SoC in 2000

Size | Cores | LP Req | Protocols | Analog
---|---|---|---|---
100x | 16x | 10x | 5x | 5x

Increasing Verification Challenge

Simulation performance?
Code coverage?

How long will verification take?
How many people are required?
What is the cost of verification?
Can the simulator handle this big design?
How to verify the software?
How to verify low power techniques?
How long does it take to debug?
When will the coverage goal be reached?
How to verify AMS designs?
VIP availability, quality, feature?
Will there be X-related problems?
???
Global Verification Survey

2 global surveys
10+ countries
2000+ respondents
Analog, Functional, System
100+M Gates SOC
Verification Requirements

Verification Closure
- Performance & capacity
- Constraints solver
- Coverage closure
- Debug

VIP
- Availability & quality
- Performance impact
- Coverage closure
- Ease of use & debug

Low Power
- LP techniques
- Performance impact
- UPF, methodology
- Ease of use & debug

Higher Level Abstraction
- TLM – RTL integration
- TLM debug
- Performance
- Ease of use & debug
VIP Usage Nearing 50%

VIP users who also use verification methodology: 69%

Verification IP in Current Design:

Do you use verification IP in your current design?

- Yes: 44%
- No: 56%

N=1256
VIPs: Next Verification Abstraction
New Verification IP Architecture

**Accelerate Time to Results**

- QuickStarts
- VIP Configurator
- Env Builder

- SV-based
- Optimized code
- Config-Optimized

- Built-in Coverage
- Test Suites
- Sequence Builder

- Visualization
- Intelligent Visibility
- Protocol Analyzer
Protocol Analyzer

✓ Browse Protocol Activity
✓ View Docs and Class Reference Hierarchy
✓ Quickly identify problems and causes
✓ Linked to Debug
Easy Integration With Debug

✓ Linked PA Time/Zoom
✓ Separate PA cursors
✓ Autoload VIP signals
Extensive Built-in Protocol Functional Coverage and Test Plans

- **Test Plan**
  - Derived from specification

- **Automated back-annotation of coverage results**

- ✔ Minimizes protocol knowledge
- ✔ Jump-starts testbench development
- ✔ Lets you know when you are done

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SoC Development Costs

- Typical 12 month design cycle from specification complete
- One metal mask spin required
- 6 month customer and field qualification post 1st silicon

Source: IBS, Synopsys
Virtual Prototyping

Pre-Silicon SW Development

SW-Driven Verification

System Validation

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Virtual Prototype - RTL
5x faster verification combined TLM/RTL

**TLM Model**
- Complete system model
- Extreme simulation performance
- Large TLM library

**RTL Model**
- TLM interface
- Layered Methodology
- Transaction-level models in SystemC or SystemVerilog

**Simulation runtime (mins) for ARM-based wireless system**

Source: Leading Wireless Company (2010)
Reference Model in SC

Scenario → Function → Command → HDL DUT → Monitor → Transaction Level Interface

SystemC

Testbench

Scoreboard

SC, SC-SV TLI, PIN IF, SV-SC TLI, SV, Channel/Socket

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SV Testbench for SC Model
TLM-2.0 Across SV/SC
TLM-2.0 Bridge Between SV & SC

- Proxy sockets terminate the TLM2 connections in each language
  - Create SV/SC bridge
Avoid RTL (Re-)Verification

Formal Block-Level Consistency Checker

- Proves consistency of independently developed models
- Exhaustively verifies successive design refinements
- Does not require testbenches, assertions, coverage
Product Verification
Accelerated Time-to-Market

Traditional System Development

- SW Development
- HW Development
- Integration & Test
- Product Support & Maintenance

With Methodology, VIP and Prototyping

- SW Development
- HW Development
- Integration & Test
- Product Support & Maintenance

Less Effort

Earlier TTM