Top3 Verification Challenges

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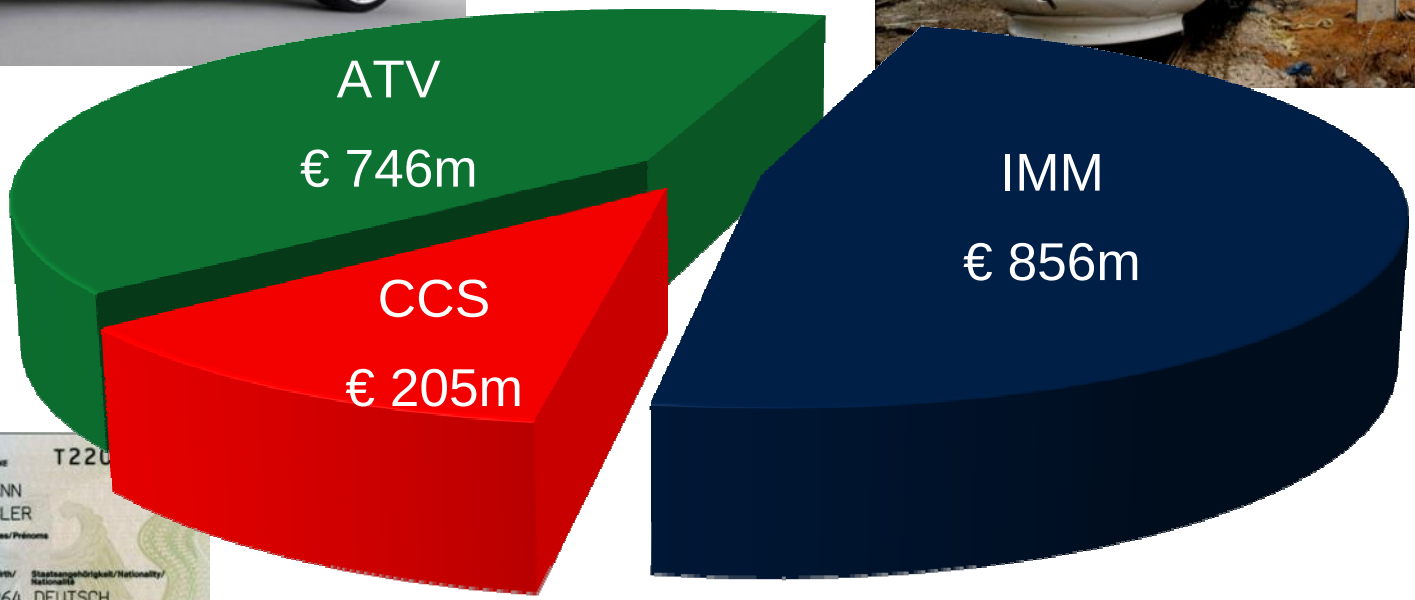
Infineon - Revenue Split by Division

6-months FY11 revenue split



Infineon Automotive Semiconductor Solutions Combine **Sense**, **Compute** and **Actuate**

Our target markets	Sense	Compute	Actuate
Powertrain  ■ Diesel Engine Mgmt. ■ Gasoline Engine Mgmt. ■ Transmission Control ■ Starter / Alternator	■ Pressure Sensors ■ Magnetic (Hall) Sensors #1	■ 16/32 bit µC ■ 32 bit TriCore® (µC + DSP) #2	■ MOSFETs #2 ■ IGBTs ■ Regulators ■ Transceivers #2 ■ Smart Power ■ System ICs
Hybrid Electrical Drives  ■ Hybrid motor drive ■ Regenerative braking ■ Battery management	■ Magnetic Sensors	■ 8 bit µCs ■ 16/32 bit µCs ■ 32 bit TriCore® (µC + DSP)	■ HybridPack #2 ■ IGBTs #1 ■ Regulators #1 ■ Transceivers #2 ■ Smart Power ■ MOSFETs
Safety  ■ ABS/ESP/Traction Control ■ Suspension ■ Airbag/Restraint Systems ■ Side-airbag ■ Power Steering ■ Tire Pressure Monitoring	■ Pressure #1 ■ TPMS #1 ■ Magnetic (Hall) Sensors #1 ■ RF ICs #1	■ 8 bit µCs ■ 16/32 bit µCs ■ 32 bit TriCore® (µC + DSP)	■ Diodes ■ Transistors ■ MOSFETs #2 ■ Regulators ■ Transceivers #2 ■ Smart Power ■ System ICs
Body & Convenience  ■ Light Control ■ Heating, Ventilation, Air Condition ■ Door & Seat ■ Smart Battery Terminal	■ Magnetic Sensors #2 ■ RF ICs #1	■ 8 bit µCs ■ 16/32 bit µCs	■ Transceivers #2 ■ Diodes ■ MOSFETs #2 ■ Transistors ■ Regulators #1 ■ E-Power ■ Smart Power #1

Our Top3 Verification Challenges

- **Top1**: **Mastering Verification Complexity**
  - Continuous increase in number of IP's and embedded processors
    - 2006: 30-40 IP's, 1 CPU
    - 2011: 80+ IP's, 6+ CPU's
    - *2016: 120+ IP's, 20 CPU's ?*
  - The more IP's the higher the risk of late spec & implementation changes
  - Driving towards true Hw/Sw Co-Verification
  - Reuse of verification environments / stimulus from IP-level into big multi-CPU SoC environments

Our Top3 Verification Challenges

- **Top2**: **Debug Automation**
  - Managing data complexity
    - 100's of MBytes of Waveform, Logfile, Trace Data make it difficult to get quickly to the root cause of problems
  - Keeping track of IP-versions/changes/fixes/bugs
  - Proper balancing between high-speed simulation and high-detail visibility
    - Add additional checkers/loggers etc. only when needed
  - Determination of the cone-of-influence for failures
    - 6000+ pages of functional specification are difficult to map to all functional scenarios seen in simulation

Our Top3 Verification Challenges

- **Top3**: **Requirements driven verification / validation**
  - New “ISO26262 Road Vehicles — Functional Safety“ Standard requires full traceability for verification/validation plans from *Spec→IP → SubSystem → SoC → Complete Hw/Sw-System*
  - Manual feature tagging difficult to maintain in case of changes
  - Proving validity of feature tags by backannotation of completion metrics such as coverage

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