Formal Contribution towards Coverage Closure

Deepak Pant
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Agenda

1. Incisive Metric Driven Verification
2. Coverage Unreachability App
3. Enriched Metrics – Formal Contribution to MDV
4. Summary
Incisive Metric-Driven Verification (MDV)

Use Enterprise Planner to bind assertions’ and checks’ goals to features; generate the vPlan

Write new assertions, or use Assertion Based VIP

Contributions from multiple technologies shown in a unified view

Run formal or dynamic assertions in parallel

Plan

Construct

Execute

Measure / Analyze

Spec

Design Specification

output_ready:assert property ...

UniCov DB

IFV/IEV

IES-XL

HW
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Verification Apps Across the Project Life Cycle

- RTL Design
- RTL Refinement
- Testbench Development
- IP Verification
- Integration

**Designer**
- Project Start
- RTL partially available
- Testbench Ready
- Feature/Protocol Finished
- Verification Closure
- System Tapeout

**Verification Engineer**
- Super Linting
- Protocol Compliance
- Coverage Unreachability Analysis
- Register Map Validation
- SoC Connectivity

**System Integrator**
- RTL Design
- Verification Apps Across the Project Life Cycle

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module multiplexor4_1 (out, in1, in2, in3, in4, cntrl1, cntrl2);
  output out;
  input in1, in2, in3, in4, cntrl1, cntrl2;
  reg out;

always @(in1 or in2 or in3 or in4 or cntrl1 or cntrl2)
  case ({cntrl1, cntrl2})
    2'b00 : out = in1;
    2'b01 : out = in2;
    2'b10 : out = in3;
    2'b11 : out = in4;
    default : $display("Please check control bits");
  endcase
endmodule

Question:
Is the uncovered code reachable or unreachable?

Test suite is insufficient. BAD!
Fix RTL or discard hole. OK!
The Coverage Hole Problem

- Run simulation and collect metrics
- Review metrics in IMC
- Uncovered items → Create more tests!

Question: Is the uncovered item reachable or unreachable?
Coverage Unreachability App Overview

- Leverage formal to determine if “holes” are reachable
  - Block code coverage
  - Expression code coverage
- **But:** automated flow – no formal/ABV knowledge required!
- **And:** Independent of testbench methodology!
Results Handling

• Only unreachable holes are reported
• Merge unreachable database into original simulation database
Result Reviewing

- Read in merged database (simulation + unreachable)
- User to accept UNR by converting into Exclude
- RESULT: Enhanced code coverage as elements found to be unreachable are now annotated as Exclude
Customer Feedback

• Successful adoption at multiple customers

• Feedback and impressions
  – Easy to use
  – Good performance
  – *Saves a lot of review cycles for hole analysis*

• Tech. paper: Freescale Bangalore at CDNLive! India
  
  
  > I. Silicon Realization: Functional Verification
  > Session 1.6 : Innovative Approach To Coverage Closure Through Unreachability Analysis Flow
Fujitsu Article in EETimes


Using code-coverage analysis to verify 2D graphic engines in automotive apps

Florian Mueller

20 June 2012

High-resolution graphics displays are becoming a key part of automotive manufacturers’ strategies to simultaneously differentiate from their competitors, reduce production cost, and increase customer satisfaction. Our group at Fujitsu develops IP blocks and SoCs to help customers realize these advantages.

One of our IP blocks is called Iris, a 2D graphics engine. This IP is of many reusable sub-components, which can be easily rearranged into derivatives. It is then integrated into a range of product lines. These sub-components, of course, need to be verified in addition to the product. For this purpose, we employ a metric-driven verification flow.

Conclusion

As previously stated, the automatic code coverage analysis by Incisive Enterprise Verifier is very simple to set up and execute. In our case, we integrated it into our template verification environment; so every verification engineer will have it available without any additional effort (unless they decide to use initialization). So for us, the effort necessary to utilize the automatic analysis is small compared to the gain from saved review time. We recommend that you give it a try.

Florian Mueller (Florian.Mueller@de.fujitsu.com) is a design engineer at Fujitsu Semiconductor Europe (FSEU). He is responsible for top-level design, integration, and signoff on his 2D graphic subsystem and is also participating in sub-module design and verification.

http://emea.fujitsu.com/semiconductor
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Enriched Metrics

Incisive Enterprise Verifier

Dynamic Simulation

Formal Engines

Formal & Dynamic sim results automatically annotated to the “vPlan”

- Verify formal assumptions
- Highlight unreachability
- Take credit for formal work
Report Functional Unreachables

Simulation coverage hole – But can it be reached?!?!

Formal says NO!
UVM + IEV = Multi-Engine UVM

- Create “Passive” Test
- Replay all formal witnesses in the PASSIVE UVM environment
  - Formal contributes
    - Scoreboard failures
    - Covergroup filling
    - Code coverage
    - Etc
- Bring results together using EMGR
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Summary

• The Coverage Unreachability App automates post-simulation coverage hole analysis
  ➢ TB and DUT independent
  ➢ Minimal tool knowledge is required
  ➢ Reduces time to verification closure

• Unreachables can be analyzed or removed from the master RTL/coverage database

• Easy to setup, quick to run, increases overall productivity

• Formal MDV & Coverage Unreachability – a key tool for Coverage Closure

**Bottom Line**

*Formal MDV & Coverage Unreachability – a key tool for Coverage Closure*
Documentation and Webinars

- Incisive Enterprise Verifier User Guide
  Chapter 5: Analyzing Unreachable Coverage
  <root>/doc/ievuser/ievuser.pdf

- Archived webinars
  - Formal Apps to Automate Mainstream Verification Challenges
  - What to Do When Code Coverage Closure Seems Impossible