



Reuse – Key for Mitigating IP Verification Challenges

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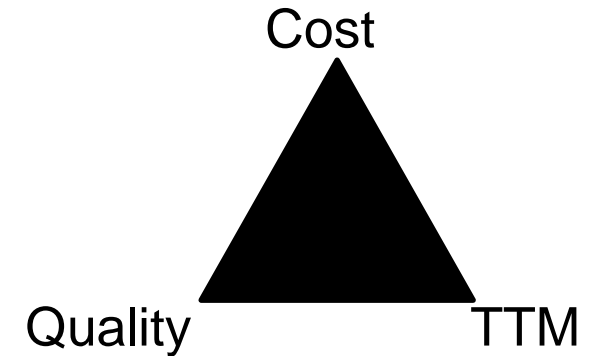


Agenda

- IP Verification Goals and Approach
- VIP Challenges
- Developing Inhouse Verification infrastructure
- Summary

IP Verification

- Goal
 - Reduce the engineering effort
 - Tradeoff between Quality, Cost and Time to market(TTM)



- Approach
 - Pre-verified Hard or Soft IP
 - In-built Verification infrastructure



VIP Challenges

- Pre-verified Hard or Soft IP
 - IP Provider Challenges
 - UVM adoption
 - Reuse, Interoperability, Configurability
 - Support for other platforms – ex: System C, Emulation, etc
 - Horizontal and vertical reusability
 - Multiple clients with different requirements – Configuration explosion
 - Simple user interface for configuration
 - Meet all functional and performance requirements
 - Can we reuse Verification IP at the Chip level?

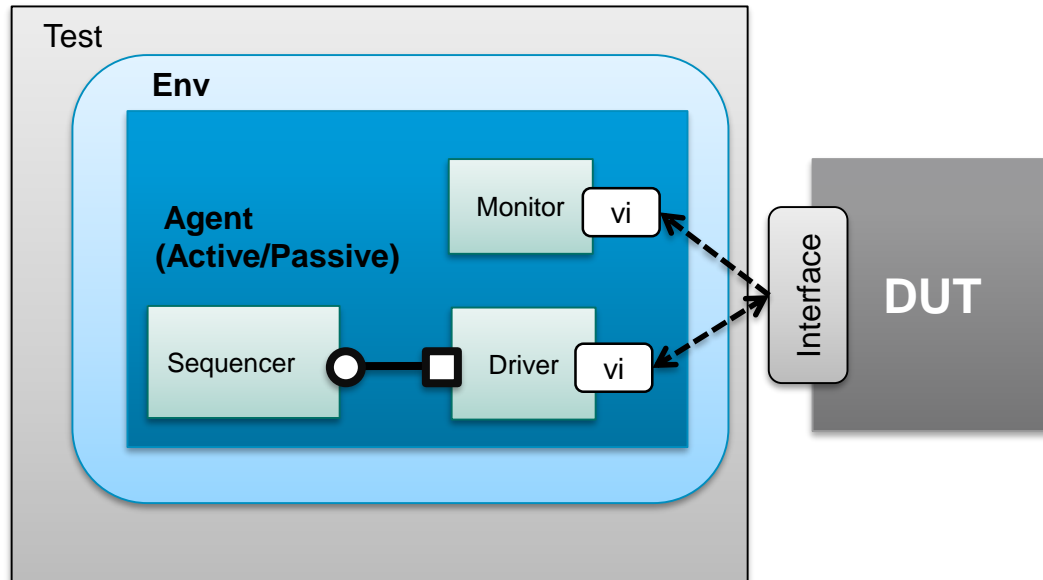
IP Verification

- Pre-verified Hard or Soft IP
 - IP Consumer Challenges
 - Quality of the IP and support system
 - Verification process, Methodology, tools
 - Detailed documentation, FAE and timely engineering support
 - Support for Coverage – Functional, Code
 - IP integration and Debug

Developing IP Verification Infrastructure

- Re-use is the key
 - UVM widely accepted as industry standard
 - Methodology for developing infrastructure
 - Identifying block level and Chip level features
 - Horizontal and Vertical Reusability
 - Easy to Configure and Integrate
 - Interoperability – TLM
 - Quality metrics – Coverage

Typical UVM Environment



Summary

- Do I choose standard VIP or Develop Inhouse?
- Standard VIP
 - Reduced TTM, More Cost and Rigid
- Develop Inhouse
 - More TTM, Moderate Cost and Flexible



**Planning and
Reuse**

Acknowledgement

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Thank You





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