Debug with Emulation

Revealing what’s not visible with simulation
What is Emulation?

› Programmable hardware built with programmable logic (FPGA) and programmable interconnect devices (PID)

› Software which automatically programs the hardware according to the circuit under design

› Control HW/SW to support operation of the emulated design as a hardware component operating in real time
Why Emulation?

![Diagram showing Bug Detection with Emulation, Simulation, and Bugs Detected lines. Days, Weeks, Months, Yikes! axes.]

- Emulation
- Simulation
- Bugs Detected
Hardware Debugging

- Debug probes – 100% signals visibility
- Breakpoints & Triggers
- Clock control
- True RTL debugging
- Memory visibility
Debug Probes

- **Static Probes** with multi-chip embedded logic analyzer
- **Dynamic Probes** – 100% visibility with Xilinx Readback and visibility debug
- **True RTL view** in various tools (ASDB, FSDB, VCD support)
- **Automated RTL code instrumentation** before synthesis
Static Probes

• Groups of probes
  • Up to 16 groups x 16 Kbit of probes
  • Selecting a working group at runtime
• Samples captured in-FPGA and transmitted via HMDB – dedicated debug bus
• Flexible buffer allocation for samples – DVM can allocate free RAMB resources for static probes
• Samples storage
  • Continuous - no drop-off mode
  • With time windows
  • Storage expression
• Sampling clock configured at runtime
• Results saved in ASDB (Aldec) or FSDB (Synopsys)
• Preserving RTL names, hierarchy paths, types
Static Probes – Triggers & Breakpoints

- Separate trigger groups
  - Up to 16 groups x 256 bits
- Triggering options:
  - Basic and advanced trigger functions
    - ==, !=
    - <, >, <=, >=
    - In-range, out of range
  - Boolean trigger expression
  - Sequence expression
  - Trigger event counter
- Breakpoints
  - Using the same trigger groups as input
  - The same functions as in trigger
  - Configured independently from triggers
Dynamic Probes

- Dynamic Probes selection at runtime
- Enhanced visibility via HVD
  - automatic design analysis and RTL instrumentation for essential probes
  - Capturing only for essential probes
  - Other signals are evaluated by HVD
- Capturing samples via Xilinx Readback (ICAP)
- Debug samples are transmitted over PCIe to Host PC
- Breakpoint on Dynamic Probes
- Configurable Sampling clock
- True RTL view
Memory Visibility

- Memory models used have a back-door interface for debugging
- Provide read & write access at emulation runtime
- Memories in emulation are identified with original RTL hierarchy paths
- Using physical addressing and data organisation to access memory contents
- Single cell and block read/write
- Viewer with configurable data formats
  - Little/big endian
  - Hex/bin radix
  - ASCII format view
- Convenient for program and data memory initialisation in SoC bring-up
HWDebugger Tool

- Provides a GUI for all emulation debugging functions.
- Contains scripting commands for automation.
- Connects to emulation target using a TCP/IP socket.
The **Debug API** is a library with interface in “C” that can be used in any application capable of linking C or C++ objects.

- C-API easily integrated with any testbench or application (C, C++, SystemC, SV DPI-C, Tcl, Python)
- Enables white-box testing methodologies for emulation
- Direct access to debug probes and memories in emulation
- Fast interface for demanding applications
Embedded Software Debugging

Example of SoC co-emulation with Virtual Platform

- **In Virtual Platform**
  - VP vendor provides interface

- **In Emulator**
  - vJTAG transactor and debugger interface library with TCP-IP
  - Mapping JTAG or other debug ports to on-board connectors
What is HES™?

- Transactors
- Monitors
- Speed Adapters

• SCE-MI
• System Verilog, UVM
• SystemC, C++
• VHDL/VHPI, Verilog/PLI
Aldec FPGA Boards

**HES7XV4000BP**
2 x Virtex-7 LX 2000
24 Millions gates

**HES7XV12000BP**
6 x Virtex-7 LX 2000
72 Millions gates

**Backplane**
up to 288 Millions gates

Coming Soon (Q3/2016)
Xilinx UltraSCALE™ on board
Up to 633 Million gates
HES Applications & Interfaces

**In-circuit Emulation**
- Simulation Acceleration
- Co-emulation
  - Virtual Models
  - Virtual Platforms
- SCE-MI
- MI
- PLI/VHPI
- TLM

**Hardware Debugging**
- Break
- Capture
- Run

**SoC Integration**
- Software Debugging
  - JTAG Port
  - vJTAG Xtor

**TCP-IP**

**SCE-MI**

**HES™**
Conclusion

- Emulation is becoming more popular and affordable
- Full simulation of SoC is not always possible
- Danger of not ‘seeing’ bugs due to simulation length
- Emulation can reveal bugs that simulation cannot ‘see’
- Comprehensive hardware debugging exists
  - Static probes
  - Dynamic probes
- Full signal visibility and correlation with RTL
Corporation Headquarters
2260 Corporate Circle, Suite 400
Henderson, NV 89074
Ph +1.702.990.4400
Fax +1.702.990.4414
sales@aldec.com

Aldec Europe
Ph +44.1295.201240
sales-eu@aldec.com

Solutions
Riviera-PRO™
Advanced Verification Platform
Active-HDL™
FPGA Design and Simulation
ALINT-PRO™
Design Rule Checking
HES-DVM™
HW/SW Validation Platform
Spec-TRACER™
Requirements Lifecycle Management
DO-254/CTS™
FPGA Level In-Target Testing
HES-7™
SoC/ASIC Prototyping
RTAX/RTSX
Prototyping Microsemi™ Rad-Tolerant Devices

Training
https://www.aldec.com/training

Support
https://www.aldec.com/support

Blog
https://www.aldec.com/company/blog

LinkedIn
YouTube
RSS
Twitter