FPGA accelerated IP validation

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FPGA technology in ARM®

- Simulation and Emulation don't scale when verifying large multi-core, multi-cluster compute sub-systems
- The aim of the FPGA group in ARM is to provide hardware accelerated verification capability to ARMs IP verification engineers
- Running multiple FPGA platforms at speed and in parallel we achieve cycle counts equivalent to running in silicon for extended periods
- High levels of debug visibility - >1K signals per FPGA and with the use of Read-Back we enable non-FPGA engineers to use FPGAs to run the debug process on hardware
- We provide remote access to hardware farms that enable non-FPGA engineers to run and debug large test payloads

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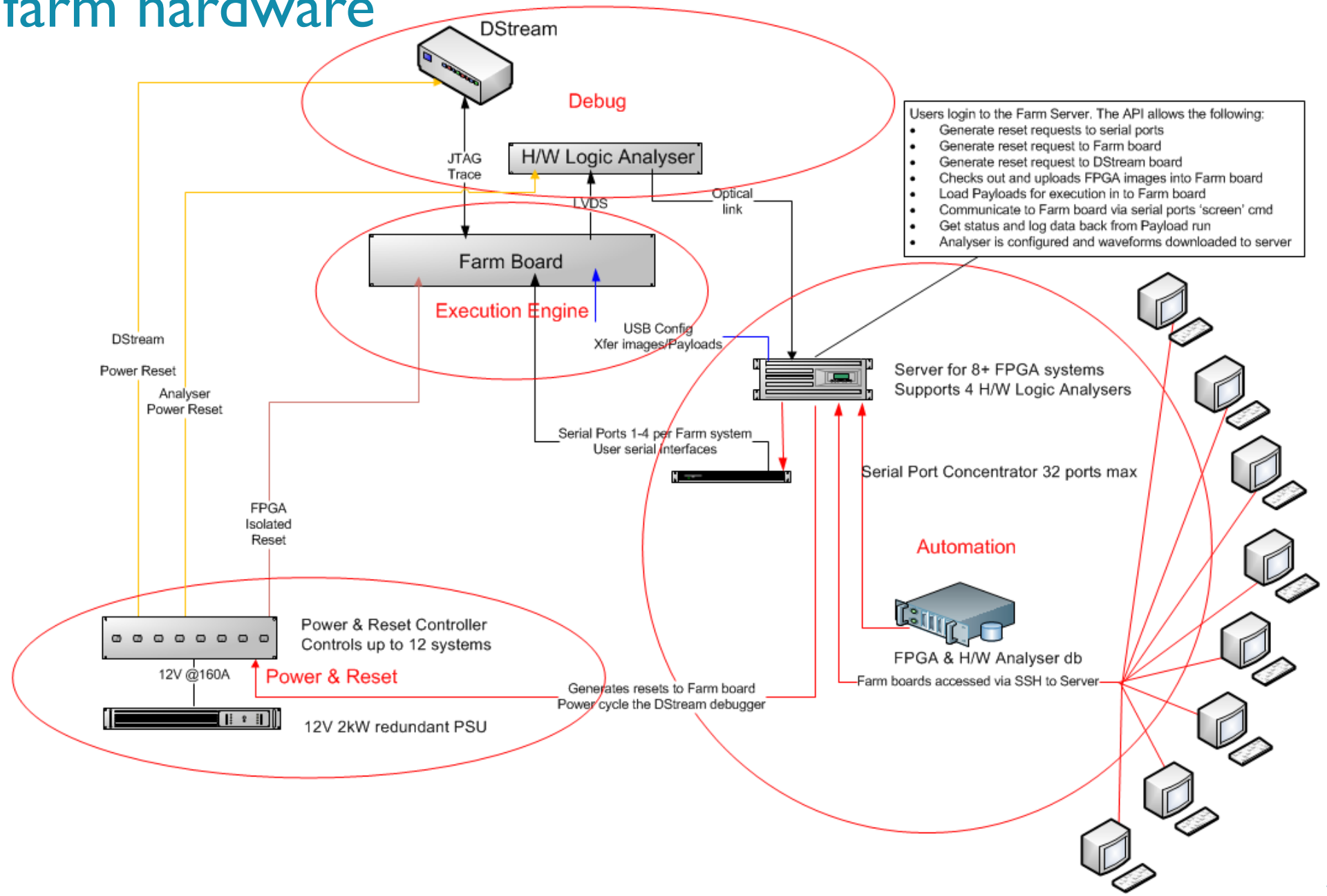
FPGA farm hardware



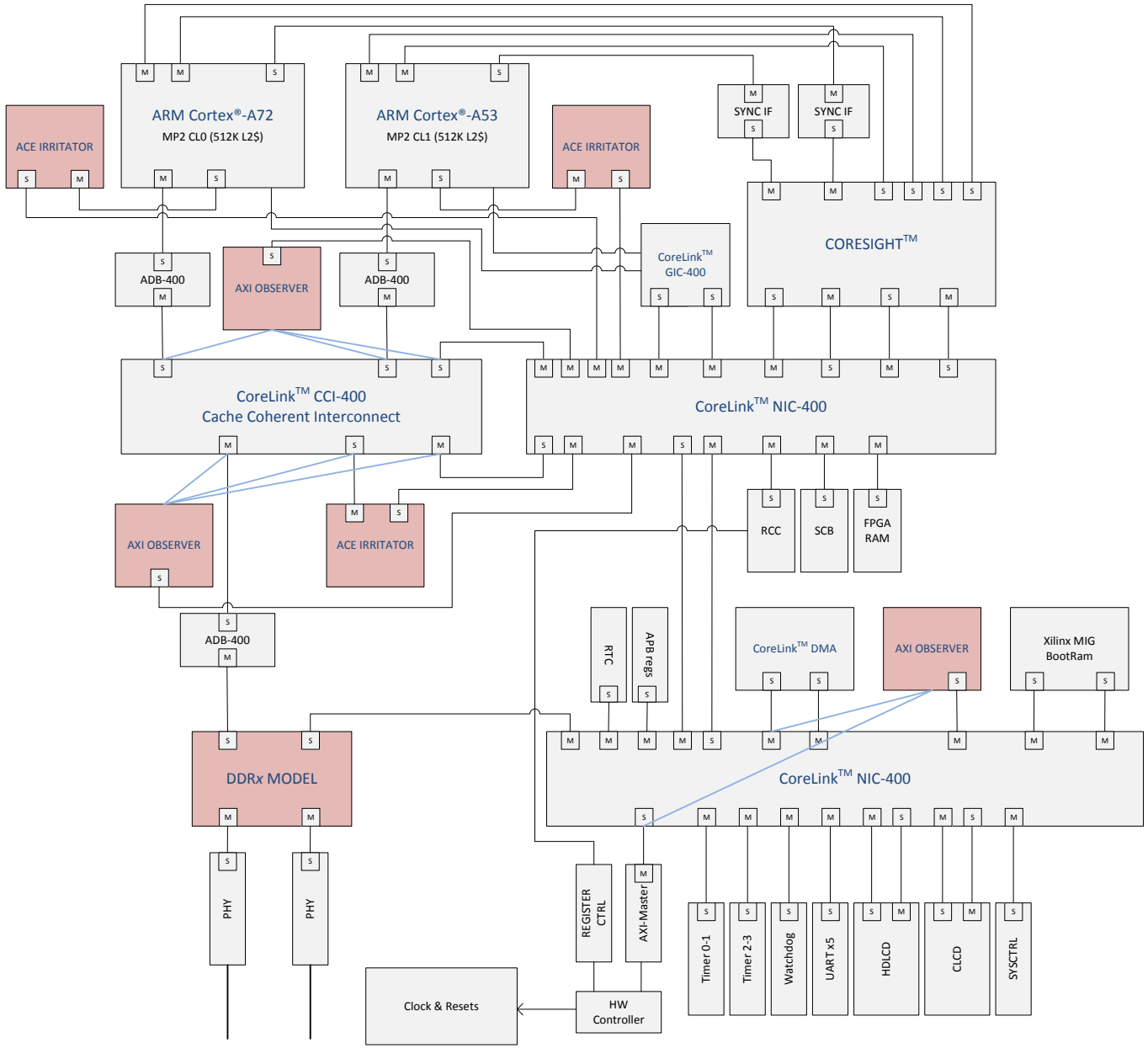
Three Requirements

- The right system
- The right stimulus
- The right debug

The Right System

- A rarely observed bug is rarely fixed
- To repeatedly observe a failure a cycle accurate system is key
- All sources of asynchronous behaviour must be identified and removed
- Clock domains
  - Run synchronously
  - Representative clock rates
- External stimulus must be controlled or removed altogether
- Verification IP is critical to creating stress in the system and to identifying faults
  - Protocol checkers – key to identifying bugs
  - Memory Models – representative clocking & cycle accuracy
  - Coverage checkers – feedback to the IP verification leads
  - Irritators – to create stress & flush out hard to find bugs

Typical FPGA validation system



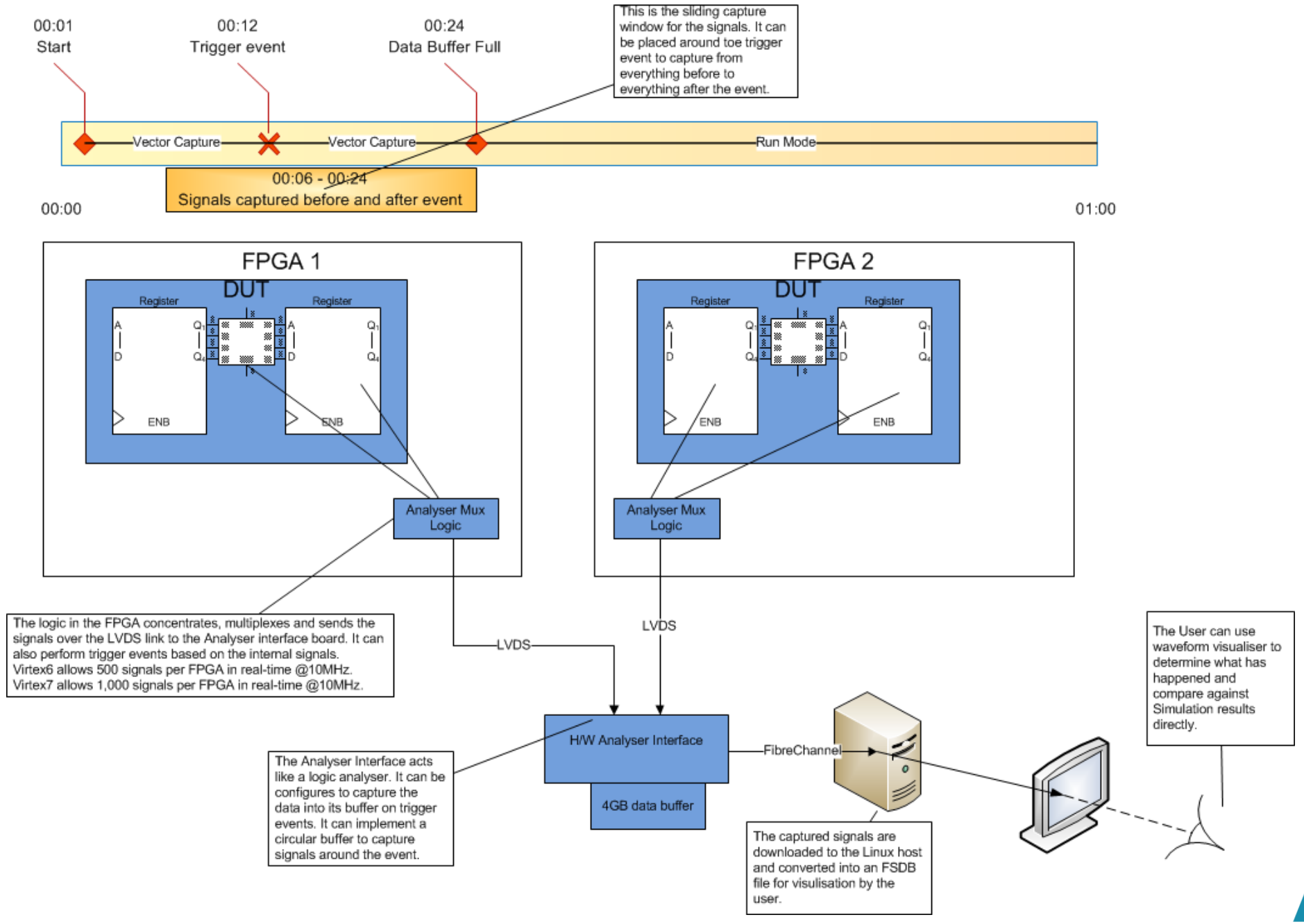
The Right Stimulus

- Make the best use of every cycle
- Self generating stimulus capable of running indefinitely on the DUT
- A mixture of directed random and full random stimulus
- Able to control traffic throughput with the use of hardware irritators
- Verification IP accompanying the stimulus actively monitors the state of the system during testing
- Short regression tests derived from running months of stimulus
- Bus monitors provide coverage feedback to provide feedback to stimulus designers

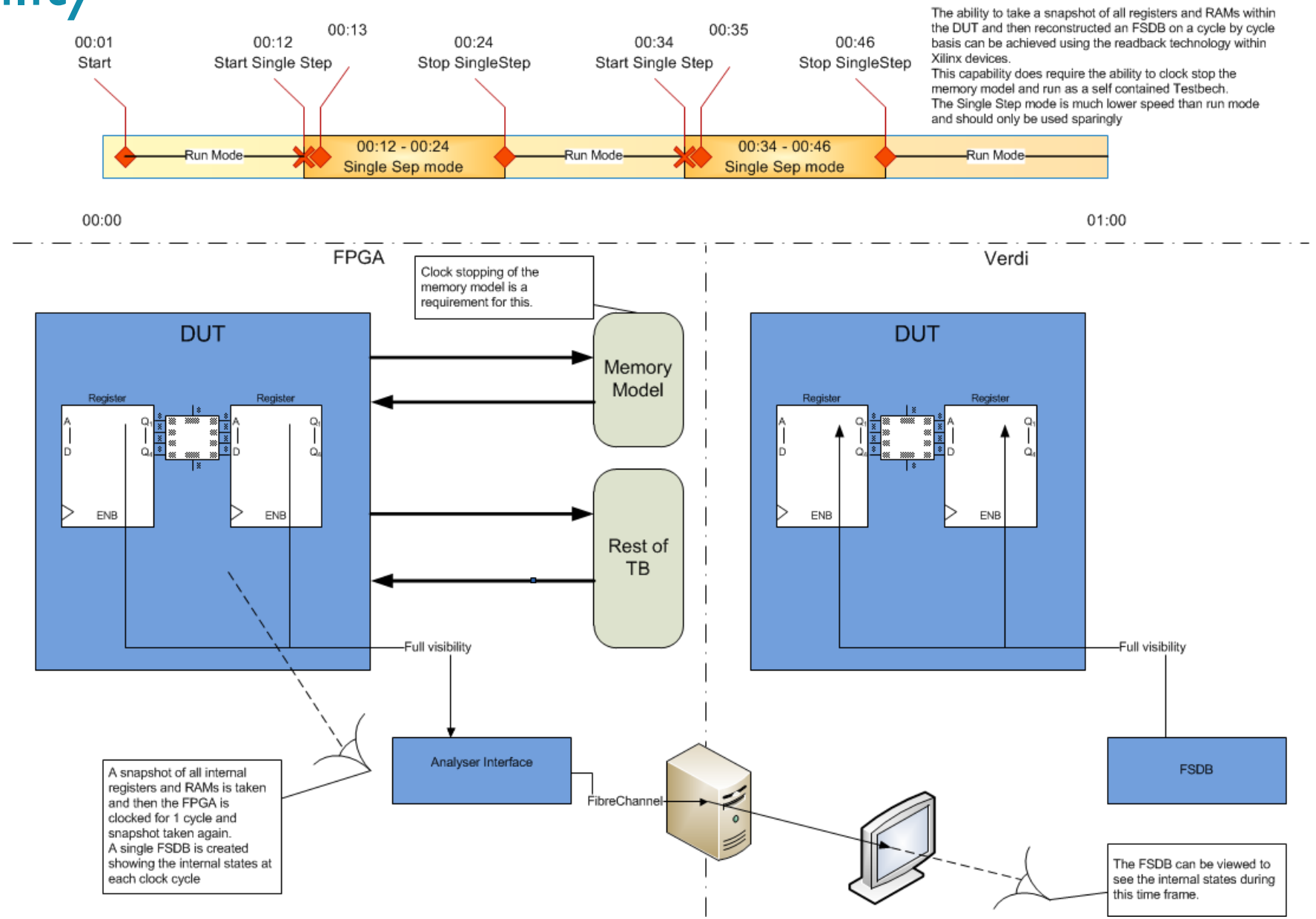
The Right Debug

- Without the ability to debug issues there is little point in running on FPGA
- Traditional software debuggers used alongside an embedded logic analysis system
- Visibility of at least 1,000 signals per FPGA with external data buffering
- Rarely are the debug resources correctly focused to root-cause a failure first time round
- Implementation flows to allow non-FPGA engineers to re-target the debug to interesting points in the system
- Read back to get full view of the design
- Clock control to build up full picture over prolonged period

Probing


00:01
Start
00:12
Trigger event
00:24
Data Buffer Full
This is the sliding capture window for the signals. It can be placed around toe trigger event to capture from everything before to everything after the event.
Vector Capture
Vector Capture
Run Mode
00:06 - 00:24
Signals captured before and after event
00:00
01:00
FPGA 1
DUT
Register
Register
ENB
ENB
Analyser Mux Logic
FPGA 2
DUT
Register
Register
ENB
ENB
Analyser Mux Logic
The logic in the FPGA concentrates, multiplexes and sends the signals over the LVDS link to the Analyser interface board. It can also perform trigger events based on the internal signals.
Virtex6 allows 500 signals per FPGA in real-time @10MHz.
Virtex7 allows 1,000 signals per FPGA in real-time @10MHz.
LVDS
LVDS
H/W Analyser Interface
4GB data buffer
FibreChannel
The Analyser Interface acts like a logic analyser. It can be configures to capture the data into its buffer on trigger events. It can implement a circular buffer to capture signals around the event.
The captured signals are downloaded to the Linux host and converted into an FSDB file for visulisation by the user.
The User can use waveform visualiser to determine what has happened and compare against Simulation results directly.

Full Visibility



Results

- Significant numbers of erratum found in pre-release IP.
- Erratum found in released IP, not yet identified in any other environment.
  - Bugs may be observed in user Si after significant periods of time but most will never be identified or fixed
  - FPGA based testing gives the bulk cycle capacity required to observe many of these bugs as well as giving the environment in which to triage and debug them
- FPGA based testing is an essential part of all IP validation work at ARM®
- NEXT STEPS
  - FPGA stimulus on silicon
  - Methodology to catch silicon failures in FPGA

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Questions?

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