Hardware Validation Using Compiler Regression Testing

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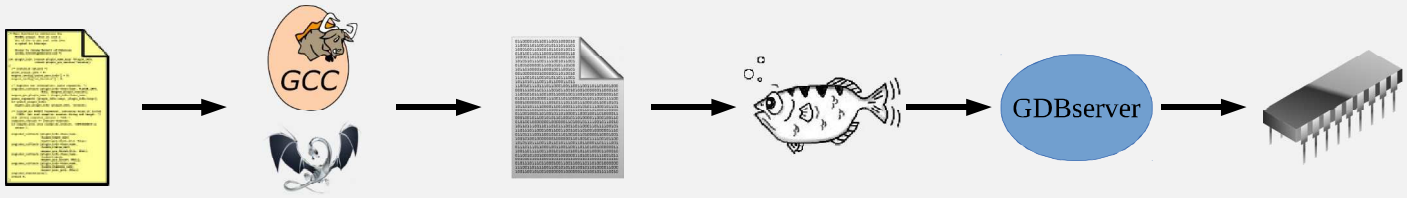
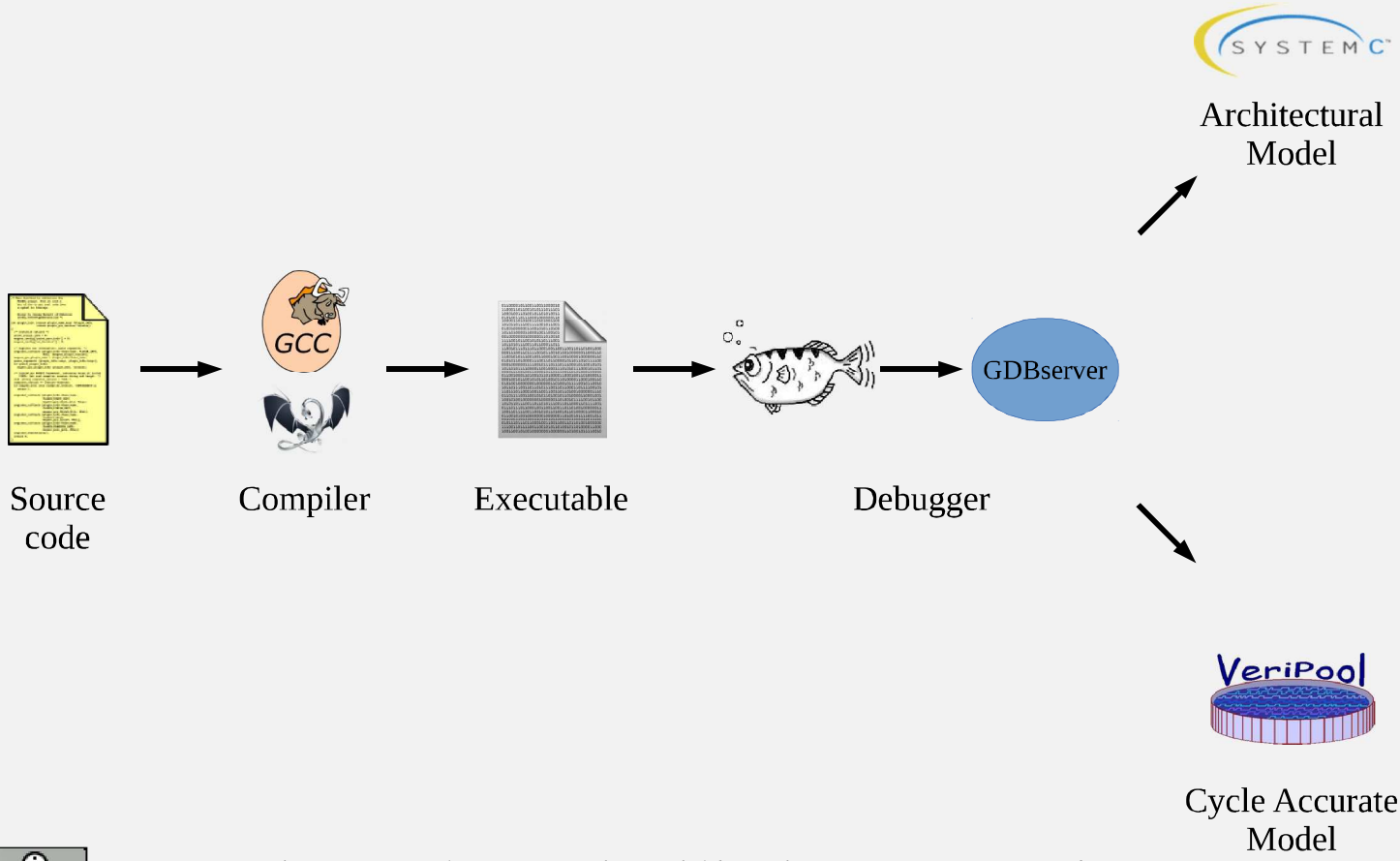
Running a Software Test



Source code → Compiler → Executable → Debugger → Chip

Running a Software Test Pre-Silicon



Comparative GCC Regression Testing

Golden SystemC TLM Model

```
                === gcc Summary ===

# of expected passes            52753
# of unexpected failures        152
# of expected failures          77
# of unresolved testcases       122
# of unsupported tests          716
```

Verilator SystemC RTL Model

```
                === gcc Summary ===

# of expected passes            52677
# of unexpected failures        228
# of expected failures          77
# of unresolved testcases       122
# of unsupported tests          716
```

- We can identify two types of problem
  - tests which fail due to timing out with RTL, but not due to slower model
  - tests which give a different result with RTL
- Used commercially by Adapteva Inc
- Modern GCC has 75k C tests and 50k C++ tests
  - next candidate for testing: RISC-V

Thank You

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