Our Story

- Tessolve established in Bangalore
  - 50,000 ft² facility with test floor, characterization lab and FA lab

- Expansion into PCB Design
- Established Tessolve Singapore

- Added IC Design services to provide full chip development solution
- Hero Electronix, part of $5B Hero Group, takes majority stake in Tessolve
- Acquired TES to expand to full embedded systems development
- Established Tessolve Malaysia (2015)

- 2004
- 2007
- 2013
- 2016
- 2017
- 2018
- 2019

- Acquired “PCB Fab” in Malaysia
- Acquired Analog Semi IC design services
- Established Tessolve Germany and Shanghai
- Test Lab in Singapore

- Establish Tessolve Korea, Thailand, Philippines and Taiwan
- Expand test engineering services to low volume production support to all 3 locations (Singapore, Bangalore and Malaysia)
- Expand IC Design strength by 2X

- Invested in Smartscale 93K and Ultraflex
- Set up secondary facility in Bangalore
- Expanded reliability lab to include HAST, Temp Cycling and THB

END-to-END PARTNER
GLOBAL PRESENCE
1800+ EMPLOYEES
25% CAGR

PARTNER
GLOBAL PRESENCE
1800+
EMPLOYEES
25% CAGR
**TESSOLVE in The HERO GROUP**

- **HERO Group** One of the most respected business houses in India since the 1950’s, delivering outstanding products & services

- **Across more than 6 industry:**
  - Automotive & Auto Components
  - Financial Services
  - Renewable Energy
  - **Electronics & IT Enabled Services**
  - Higher Education & Training
  - Real Estate

- **Hero MotoCorp** (Formerly Hero Honda Motors), the group’s flagship company, is the world’s largest manufacturer of motorcycles - **8 Million units/year**, based in India.

- Revenue: **+5B$** (Value **+15B$**)
- Total Employees: **30,000+**
Tessolve Solution: From Chip Design to Productization

IC DESIGN

TEST & PRODUCT ENGINEERING

PCB

SYSTEM LEVEL TEST

EMBEDDED SYSTEMS

Logic design
Design for Test
Design Verification
Analog Design & Layout
Physical Design & Signoff
Emulation Services

ATE Boards
System/Eval Boards
Simulation (SI/PI/Thermal)
CAM Engineering
Library Development

Functional Validation of DUT
SW + HW Integration & Testing
Test SOCs in automated environment
Bench Characterization

Yield Analysis: GRR,
Drift Analysis, Bin Flip check, Failure Trends
RMA Support
Process Improvement & Cost reduction
Test Time Reduction

Processing: ARM, MIPS, Media Processors, DSP and FPGA
Display: LCD, Capacitive / Resistive touch
Interfaces: HDMI, WiFi, Bluetooth, PCIe, SATA, Gig Ethernet
OS: Android, Linux, Windows, WinCE

Test Strategy
NPI
Platform Conversions
Characterization
Bench to ATE Correlation

Test Time Reduction

START PROCESS

END PROCESS

Tessolve Confidential
SOLUTION: INFRASTRUCTURE

PCB MANUFACTURING
• 54,000 ft² facility
• Layers: 1-30
• ISO 9001: 2008
• Capacity - 100,000 ft²/month

CHARACTERIZATION LAB
• Oscilloscope
• Logic Analyzer
• Thermal Analyzer
• Signal Integrity Analysis

TEST LAB in Bangalore, Singapore, Penang
• 50,000 ft² facility
• 13 ATE’s - V93K, Catalyst, ETS364, NI STS
• Probers - TEL P8 (8”) & UF 300 (12”)
• Handlers - Synax 141

FA and Reliability Lab
• Decapsulation
• Focused Ion Beam (FIB)
• Optical Microcopy
• Body Model (HBM)
• Machine Model (MM)
• Charged Device Model (CDM)

System Level Test Lab
• Functional Test bench
• Labwindows CVI used for Driver development and test scripts
• TestStand used for test sequences and integration with EMS
• Climatic Chamber (-40/100oC)
• Soldering Stations

TURNKEY FACILITIES
State-of-the-art test, characterization and reliability, and manufacturing facilities with complete supply chain management.

Tessolve Confidential
FLEXIBLE ENGAGEMENT

TIME & MATERIAL
- Skill-based resource
- Part of customer team

DEDICATED ENGINEERING
- Engineering team dedicated to customer
- Core team to retain skills and products
- Flex team to manage project modulation
- Necessary infrastructure (testers, servers, badge access) to meet customer requirements

REVENUE SHARING
- Partnership-based revenue sharing
- Joint ownership
- Expanded engineering capacity
- Improved cash flow

TURNKEY
- Project scope based on deliverables and managed by Tessolve
- Single front for all ecosystem
- Milestone-based payments

BUSINESS MODEL
With available resources and teams, we can engage with clients at varied levels, depending on project demands.

INNOVATION
OPERATIONS
VLSI Design

Enters the Next Level
The combined partnership will offer a full product development services with:

- Combined engineering team of 2200+
- Global support
- Local project management
- Local technical leadership
- Strong financial backing

Benefits to the customer:

- Single point-of-contact for full development
- Strong management
  - Technical leadership across the full product development
  - Project and programme management
  - Senior management relations
- Confidence in delivery
- Variety of financial engagement models
  - T&M -> SOW and delivery-based -> Shared risk
Tessolve Design Team & Expertise

**DESIGN SERVICES FLOW CHART**

- * System Specification
- * Architectural Design
- Analog Design
- RTL Design
- Design Verification
- Design for Testability
- Analog Layout
- Synthesis
- Physical Design

**Investing in People, Process and Program (PPP)**

<table>
<thead>
<tr>
<th>People: Tessolve/T&amp;VS combined No. of VLSI Engineers: ~ 700</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SOC Leads</strong></td>
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<tr>
<td><strong>RTL/Synth/STA</strong></td>
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<tr>
<td><strong>Verification</strong></td>
</tr>
<tr>
<td><strong>DFT</strong></td>
</tr>
<tr>
<td><strong>PD</strong></td>
</tr>
<tr>
<td><strong>Analog</strong></td>
</tr>
<tr>
<td><strong>Emulation / FPGA, SI Val</strong></td>
</tr>
<tr>
<td><strong>Embedded SW</strong></td>
</tr>
<tr>
<td><strong>Validation</strong></td>
</tr>
</tbody>
</table>

**Expertise**

- LP and HP Digital and Analog Designs
- RF Circuit Design
- AMS implementation of SoC and Specialty blocks, 10nm and up
- Protocols: AMBA, MIPI, PCIe, SAS/SATA, SDIO etc.

**Team Development, Retention and internal Process**

State of the art Training Center for DV, DFT, PD. Collaboration with local technical universities and state governments.

12% Low attrition compared to the industry

Target to grow team by 2X in 2019

Established Methodology for RTL, DV, PD, DFT and AMS

Established Project management and Inter-geography communication management
Why Tessolve for VLSI

Our Differentiation: A Mix-signal End-to-End Chip Solution Team

- FPGA Emulation and Post SI Validation
  Prototyping across multi platforms

- DFT & Debug
  Engineering chip anatomy with testability and debugging

- Effective Timing Closure
  Analog Digital

- Digital & Analog Design
  Agile and high quality - analog design creation

- Mixed Signal
  Agile and high quality - analog design creation

*Effective Integration
Analog Digital

*Integration and Timing Closure of Custom Hard-macros working with Digital Blocks is an art.
*An integrated analog and digital team - Supports lowest power and highest performance, and chip solution
Our IC Capability Circuitry

DFT to Analog, we chip into all with dedication

Design Verification
- Languages and Methodologies
- Protocol Knowledge
- Processor Expertise
- Low Power Verification
- Formal/Static Property based Verification
- Emulation Platforms
- Post silicon validation

Design For Test & Debug
- Multiple Clock and Voltage Domains
- Mixed signal low speed and high speed designs
- Power sensitive designs
- Embedded processor based designs
- Complex analog testing includes SERDES, DDR and A/D, D/A converters
- Experience in industry standard EDA tools
- Post silicon debug on ATE and Bench

Physical Design
- Experience in industry leading 7nm nodes.
- Experience in PDKs from industry leading fabs
- Mixed signal & Low Power designs
- High Performance designs
- Experience in industry standard EDA tools
- Closed timing in multiple process corners as per the application requirements

FPGA Emulation and Post SI Validation
- Tools expertise - Synthesis (Synplify Premier/Pro, Altera Tools), PAR & Timing Analysis (Xilinx & Altera Tools), Debug (Chip scope Altera Signal, Logic Analyzer etc)
- Simulation Tools

Analog & Mixed Signal
- Hands-on complete analog life-cycle from specs till post-silicon validation
- Expertise on SoC & block level
- Expertise on CMOS/FinFET process nodes
- High Speed AMS Design & Layout
- RF Layout
- Standard Cell Design & Layout
- Verilog, Verilog-A & VAMS modelling
ASIC Design

Skills:

- Generate micro-architecture and/or verification plan of the relevant IP
- Generate well-documented, power efficient and synthesis friendly RTL
- Debug, fix, and validate pre- and post-silicon IP/sub-system logic issues and bugs
- Familiarity with Design environment, flow, tools, methodologies and optimization methods
- Design circuits and physical implementation for IPs

Tools:

- Design: Verilog, VHDL, System Verilog
- Synthesis: Design Compiler, Genus, HDL Designer
- Linting: SpyGlass, Leda, Jasper
- Clock Domain Crossing: Spyglass CDC, Questa CDC, Jasper CDC
- Scripting: Python, Perl, Shell
ASIC Verification

Skills:

- IP/SoC Verification
- Gate Level Simulation
- Formal Verification
- SystemC Modelling
- AMS Verification
- DFX
- PHY Verification
- Verification Productivity Tools

Tools:
- Simulators – VCS, Incisive (NCSim), Questa, Modelsim, OSCI, PSpice, Fastspice, Customsim
- Debuggers – Indago, Verdi
- Formal – VC Formal, Questa Formal, Incisive Formal
- Software Driven Test – Perspec
- Planning and Metrics – vManager, Run Manager, asureSIGN
Analog Design Expertise

Power Management
- PMIC (Power Management IC)
- DC-DC Converters
- Motor Drivers (DC Brush/Brushless)
- LED Drivers (WLED, RGB LED)
- Battery Chargers
- Charge Pump, LDOs

Data Converters
- Sigma Delta Converters
- Sub-Sampling ADC
- Pipeline ADC
- Cyclic ADC
- SAR ADC
- Current Steering DAC

Serial Interfaces
- SERDES Standards
- LVDS PHY TX/RX
- CAN/LIN Transceiver
- Power Line Communications

PLLs & CLOCKS
- Integer & Fractional PLLs
- Clock Generator for SoCs
- Ring Oscillator up to 5 GHz
- Clock Buffers
<table>
<thead>
<tr>
<th><strong>Applications</strong></th>
<th>Automotive, Server, Graphics, Mobile, Consumer, Networking</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Technologies</strong></td>
<td>7nm, 10nm, 14/16nm, 28nm, 32nm, 40/45nm, 60nm, 90nm, 120nm, 180nm +</td>
</tr>
</tbody>
</table>
| **Tools**                | Cadence: Innovus, Quantus, Tempus, Voltus, Modus, PVS, Conformal LEC  
                          | Synopsys: DC, ICC/ICC2, StarRC, PT, PT-SI, ICV, Formality  
                          | Mentor: Calibre  
                          | Ansys: Redhawk |
| **Logic Synthesis**      | Logic / Physical aware Synthesis with focus on Power, Performance & Area |
| **Full Chip Level Place & Route** | Full chip level activities like IO Ring creation, Floorplanning, P&R activities |
| **Block Level Place & Route** | Block level Place & Route activities |
| **STA**                  | Multi-mode, multi-corner sign off Timing analysis & closure |
| **PV Closure**           | Sign off Physical Verification and closure of DRC, LVS, Antenna, ERC |
| **Power network analysis** | Resistance checks, Static IR drop, Dynamic IR drop analysis and closure |
| **Bump Planning, RDL Routing** | Bump placement, RDL routing of Flip Chips |
| **Flow / Methodology**   | Development / Enhancement of Physical Design flows. |
Well Balanced Team

- Team of 150 Employees.
  - 8% with > 10 years
  - 15% between 5 - 10 years
- Majority trained in Cadence tools
- Technology Experience
  - Samsung 10nm
  - TSMC 16 & 7 nm
  - GF 14 & 7 nm
  - Intel 14 & 10 nm
- Team Project Experience
  - 5G modem subsystems
  - Server CPU/chipsets, Graphic
  - Mobile processors
  - Networking, DSP cores
  - Automotive, DDR, high speed subsystems
- Team Tape-out Experience
  - ~60+ SOC tape-outs
  - ~100+ IP tape-outs
<table>
<thead>
<tr>
<th>IP/SOC</th>
<th>Technology</th>
<th>Ownership</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-core high performance</td>
<td>Samsung 10nm</td>
<td>Netlist2GDS implementation including DFT</td>
</tr>
<tr>
<td>DSP Cores</td>
<td>GF 14nm &amp; GF 7nm</td>
<td>Netlist2GDS implementation of Vision C5, P6 &amp; Q6 cores.</td>
</tr>
<tr>
<td>HSS Test chip (Contains SERDES IP from Global Foundries)</td>
<td>GF 14nm &amp; GF 7nm</td>
<td>Netlist2GDS Implementation of few blocks inside HSS test chip</td>
</tr>
<tr>
<td>Networking Chip</td>
<td>GF 14nm</td>
<td>Netlist2GDS implementation of 12 blocks (each ~2.5 Million Gates)</td>
</tr>
<tr>
<td>Automotive Chip</td>
<td>GF 14nm</td>
<td>Netlist2GDS implementation of 12 blocks (each ~2 Million Gates)</td>
</tr>
<tr>
<td>Memory Performance &amp; Standard cell Characterization chips</td>
<td>GF 14nm &amp; GF 7nm</td>
<td>Netlist2GDS implementation of four 7 mm * 7 mm chip. Involved from bump planning to GDS delivery.</td>
</tr>
<tr>
<td>Custom full chip integration flow development &amp; QA of full chip collaterals.</td>
<td>22nm, 14nm</td>
<td>Development &amp; QA of EDI, based custom full chip integration, assembly flow for 22nm. Mini die development including top level floorplan, partitioning, implementation, die ring creation, bump placements, ESD cell placements, fill flow and physical verification. Purpose was to test the full chip flow and assembly aspects of full chip collaterals.</td>
</tr>
</tbody>
</table>
### Projects Snapshot - Other references

<table>
<thead>
<tr>
<th>IP/SOC</th>
<th>Technology</th>
<th>Ownership</th>
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<tbody>
<tr>
<td>5G Modem (2 Subsystems)</td>
<td>TSMC 7nm</td>
<td>Complete RTL2 GDS implementation of subsystems.</td>
</tr>
<tr>
<td>PCIE Subsystem</td>
<td>Intel 10nm</td>
<td>Complete RTL2 GDS implementation of subsystems.</td>
</tr>
<tr>
<td>CPU2CPU interconnect Subsystem</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(3 GHz)</td>
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<td></td>
</tr>
<tr>
<td>Caching and Home agent Subsystem</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(3 GHz)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR Subsystems</td>
<td>TSMC 7nm,16nm &amp;</td>
<td>Complete RTL2GDS implementation of subsystems.</td>
</tr>
<tr>
<td>Intel 10nm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Southbridge SOC</td>
<td>Intel 14nm</td>
<td>Netlist2GDS implementation of 34 blocks.</td>
</tr>
</tbody>
</table>
Tessolve Can Setup a Centralized Design Engg Center (DEC)

Modulate Resources based on customer Needs
- RTL, DFT, DV, PD
- Test
- Board
- Product eng

Add/Remove Resource As Required by customer Needs

Core Team for Customer

Design Engineering Centre
- Industry standard office space
- Network isolation
- Internet access – VPN
- UPS, Security Camera
- Servers at Client location

Secured test floor space with badge access

Customized talent, optimized resources and cost-efficient

*DEC can be setup in B’lore, India at Tessolve facility
Tessolve DEC Infrastructure - Customer Example

- **Capacity**
  - 200 Engineer Seating

- **Connectivity**
  - Dedicated point-to-point network connectivity. Controlled by customer.

- **Teams**
  - Executing PD, DFT, DV, Analog and Product Engineering
  - SOW/KPI/milestone based projects

- **Security**
  - 24x7 Secure badge access and Camera security
  - No cell phones allowed
  - No outsiders and non-customer project Tessolve engineers are allowed access
  - No personal laptops allowed
Post Silicon Overview

- IC Design
- Test Engineering
- PCB Engineering
- System Level Test
- Embedded Systems

**SOLUTION: Post Silicon Activities**

- End to end solution for Silicon Debug/Post Silicon Validation
- From Tape out till Production Release
- And Sustaining support till end of Life of the Product

**ENGINEERING STRENGTH**

- **800+ engineers**
  - Test Development Team
  - Product Engineering Team
  - Bench Characterization Team

- **90+ engineers**
  - Post Silicon Validation Team
  - Platform Validation Team

- **170+ engineers**
  - PCB Design Engineering Team

**GLOBAL PRESENCE & INFRASTRUCTURE**

- **INDIA**
  - State of the art Test floor with different flavors of ATE
  - Dedicated ODC set up for Intel along with ATE set up
  - Characterization lab with High end bench instruments
  - Qualification lab with HTOL, ESD and LU equipment

- **MALAYSIA**
  - Office space ~4000 sqft ready with local Operations and commissioned
  - Small Scale Lab facility on ARM and FPGA setup for training and few trained resources
  - PCB fab in JB with 90+ staff

- **SINGAPORE**
  - Test floor with ATE for development and small volume production
Tessolve offers multiple platforms and testing equipment on its test floor, always manned by a team of experts provides 24/7 maintenance and operator support.

<table>
<thead>
<tr>
<th>Engineering Expertise</th>
<th>ATE Exposure</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Test Plans and Strategy</td>
<td>• Advantest V93000 SoC,</td>
</tr>
<tr>
<td>• Test Program Development</td>
<td>T6575/T6373/T6752/T2000</td>
</tr>
<tr>
<td>• Bench To ATE Characterization</td>
<td>• Teradyne: Catalyst, Eagle - ETS364,</td>
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<tr>
<td>• H/W Design &amp; Development</td>
<td>J750/MicroFlex/ UltraFlex /I</td>
</tr>
<tr>
<td>• Program Release @ OSAT</td>
<td>Flex/Tiger</td>
</tr>
<tr>
<td>• Platform Conversions</td>
<td>• National Instruments: NI STS, STS-Tx</td>
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<tr>
<td>• Production Analytics, Yield Monitoring,</td>
<td>• Focused Test FTI 1000: Power</td>
</tr>
<tr>
<td>Optimization</td>
<td>Discrete</td>
</tr>
<tr>
<td>• Device Expertise</td>
<td>• TESSPOD : 28XX series</td>
</tr>
<tr>
<td></td>
<td>• LTX Cedance: Sapphire, LTX MX, LTX-</td>
</tr>
<tr>
<td></td>
<td>C, ASL-1K</td>
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</tbody>
</table>
Device Expertise

From simple to complex to customized hardware and applications

RF
- RF Transceiver, RF Mobile Transceivers, Integrated RF Multi-band, Multi-standard receiver, RF Antenna Switches, RF Buffer ICs

Digital
- Speed & Pin count, High Speed FPGAs & SoC FPGAs, High Performance 32 Bit Digital Signal Processors, High speed Logic ICs

Sensors
- Ultra High Speed Line Scan Image Sensors, Area Scan Image Sensors, MEMS - Motion Sensor, Automotive Grade Sensors

Mixed Signal
- ADC - 16 Bit, 24 Bit & DAC, Power Architecture® Processors, PLL, Multi-Channel 24-Bit Sigma Delta ADCs.

Analog
- Analog Front End (AFE) Modules, High Speed Opamps, Precision Differential Amplifiers, Switches- Analog/Audio/Video/MIPI
Thank you for your time
Team Tessolve

TESSOLVE