Test and Verification Solutions

TVS

AMS SOC Verification

- A Practical Approach

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Agenda

- AMS Verification and Challenges
  - **Challenges with Transistor Level Simulation.**
  - **Challenges with Co-Simulation.**
  - **Challenges the AMS SOC designs pose.**
- Solution with Behavioural Models
  - **Reduce Simulation Times.**
  - **Better use of Verification Methodologies.**
- Examples of bugs found with model based flow
- Known Issues and Proposed Solutions
- Summary

AMS Design Evolution

- Need for single Chip Solutions
  - **Device Size Shrinking.**
  - **Lower Latencies.**
  - **Reduced Bill of Materials.**
- Increasing Analog design in Mixed Signal devices
  - **Not just point to point communication between Analog and Digital (E.g. Not just A/D converter and a Register update)**
  - **E.g. Low Power Designs have digital state machines which control Analog Power modules with complex handshake protocols.**

AMS Design Verification - Challenges

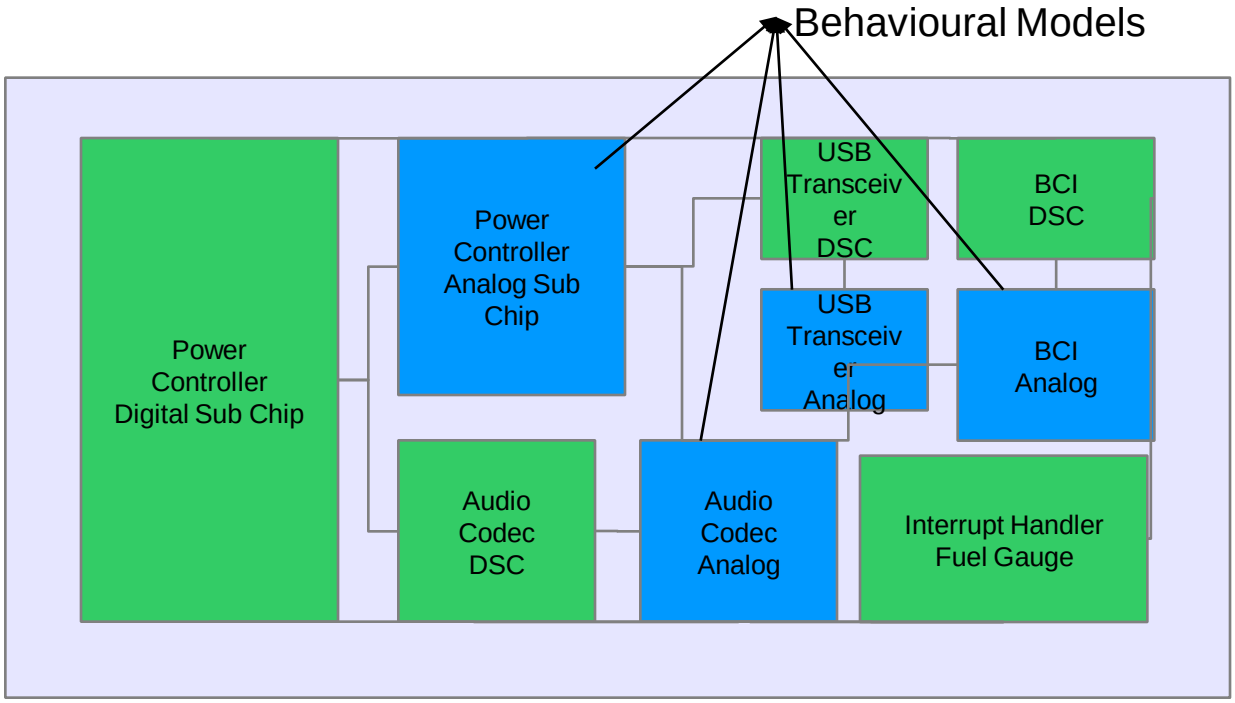
- Full Chip Transistor Level Simulations not efficient.
  - **SOC Power-up can take days to simulate.**
  - **Impractical simulation time for complex scenarios.**
  - **Verification activity delayed until analog and digital designs are close to completion.**
- Co-Simulation tools have restrictions.
  - **E.g. Spectre and ncsim**
  - **Simulation time is significantly higher compared to standalone RTL simulator.**
  - **Cost of the tool.**

What Do We Need?

- Efficient Verification Strategy
  - **Reduced Simulation Time.**
  - **Efficient Stimulus Generation and Randomization – Constrained Random**
  - **Metrics Driven Verification.**
- Identify Bugs as early as possible in the design Phase
  - **Start verification earlier**
- Cost effective solution

AMS SOC Verification with Behavioural Models

- Simulate the entire design with a digital Simulator.
  - **Replace Analog blocks with Behavioural Models**
  - **This talk will focus on VHDL models**



AMS Modelling

- VHDL used to create Behavioural models.
  - **Could use VHDL-AMS, Verilog, Verilog-AMS**
- Models can be at different abstraction levels
  - **Accuracy vs Performance and Efficiency will be the key factor.**
    - **E.g LDO Model (higher level of abstraction)**

```
supply_good <= check_power((“VBAT”, “VREF 1p5”, “IREF 1u”, “GND”),
   (vdd_in, vref_in, iref, gnd));
vdd_out <= 1.5 when supply_good and low_power = 0 else
1.4 when supply_good and low_power else infinite;
```

AMS Modelling

- The model development phase can start during architecture design phase.
  - **Can address architectural issues with simulations while design evolves.**
  - **Allows verification to have head start.**
- Can build a library of models
  - **Independent of technology**

Stimulus Generation and Automated Checking

- BFMs can be designed to drive real values.
- Analog stimulus generation models, can be controlled from e environment
  - **E.g. Signal generators can be used in the hdl test bench, and controlled by e environment to drive amplitude and frequency randomly.**
- Add checkers on the analog outputs
  - **E.g. check real value of output voltage on a voltage regulator**
  - **This is a check on the model but requires correct interaction between digital and analog**

Bugs that have been found

- Incorrect Power supply for buffer
  - **Low power domain clock buffer had higher domain power supply – No clock for digital state machine – No power up.**
- Clock Switching in digital failed
  - **Low Power clock and normal mode clock selection was relying on comparator output.**
  - **Delay in comparator output compared to the clock stop from analog.**

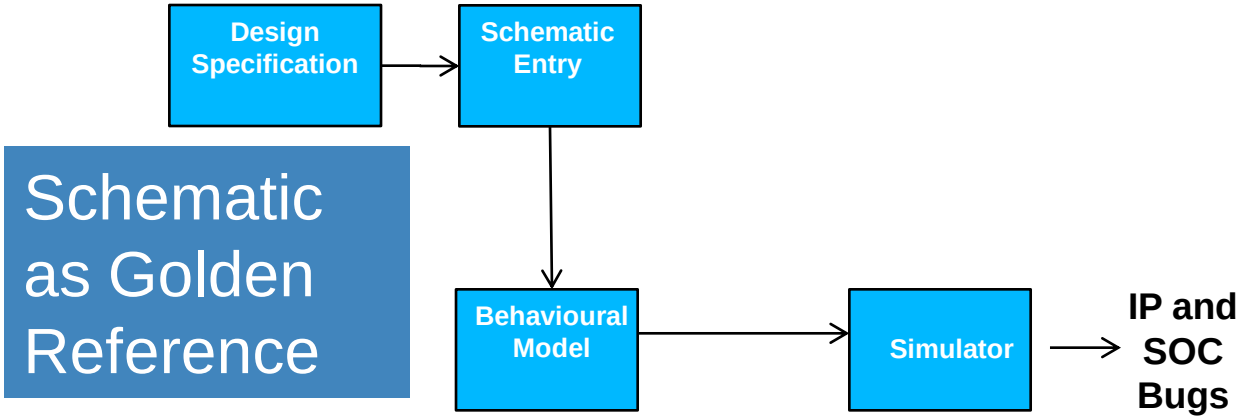
Bugs that have been found

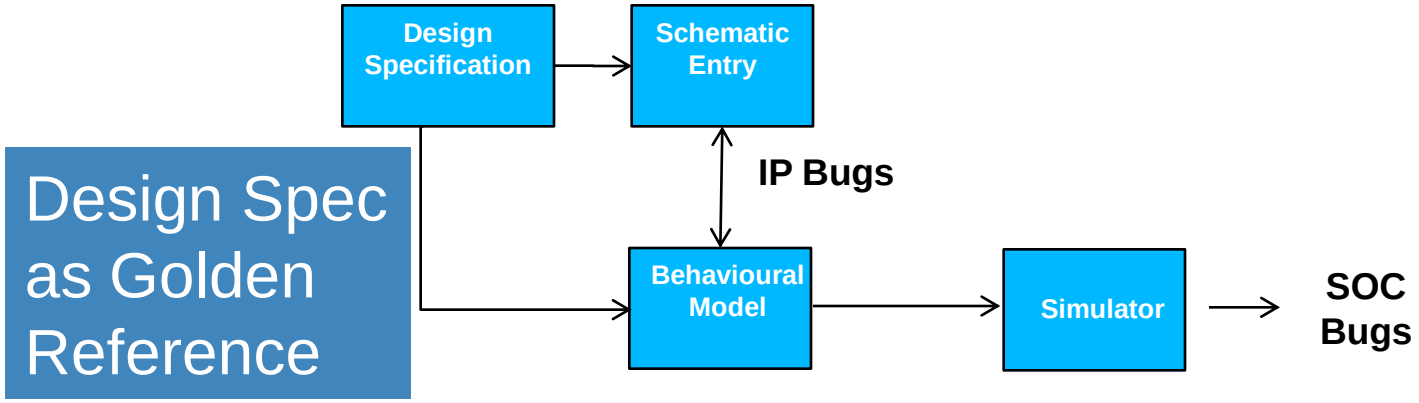
- Audio Gain Control, ADC Signals between analog and digital were swapped.
  - **If interconnections are extracted, these steps can be skipped in transistor level simulations.**

Known Issues and Solutions

- Manual Integration of blocks cannot be relied on
  - **Automated extraction is necessary to maintain the connectivity from original design.**
- Block Spice simulation results can be used to verify modelling accuracy
- What is the Golden Reference?
  - **Model development should not rely on designer word of mouth**
  - **But is Design Spec or Schematic Entry golden?**

Golden Reference?





Known Issues and Solutions

- Electrical characteristics verification cannot be done.
  - **Has to be done with block level spice simulations.**
- Modelling timing parameters for Analog block impacts simulation performance for large SOC
  - **Simulation relies on functional modelling of analog blocks.**
  - **This flow should be supported with full chip transistor level simulation of basic scenarios. (for e.g power of all blocks, configuration of gain for Audio codec)**

AMS Verification Points

- Mixed – Signal Design Interface
- Analog Blocks Connectivity
- Functional
  - **The above properties are addressed with this flow.**
- Electrical
  - **This has to be taken care at the transistor level simulations.**

Questions?