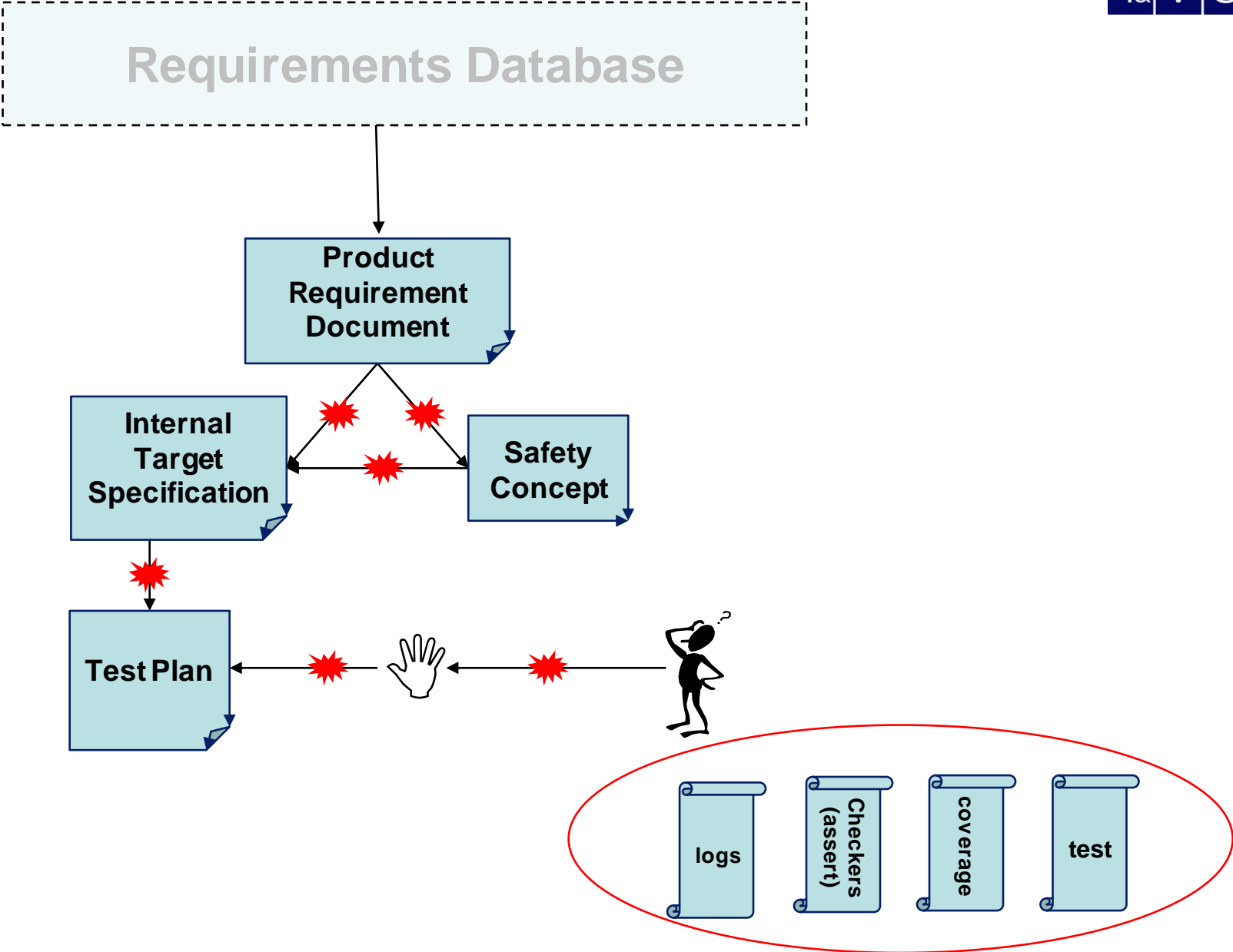


Welcome to
asureS✓gnTM

Gaurav Maheshwari
Manager Engineering - Software
Test and Verification Solutions Pvt. Ltd.

FIRST REQ ENGINEERING SOLUTION



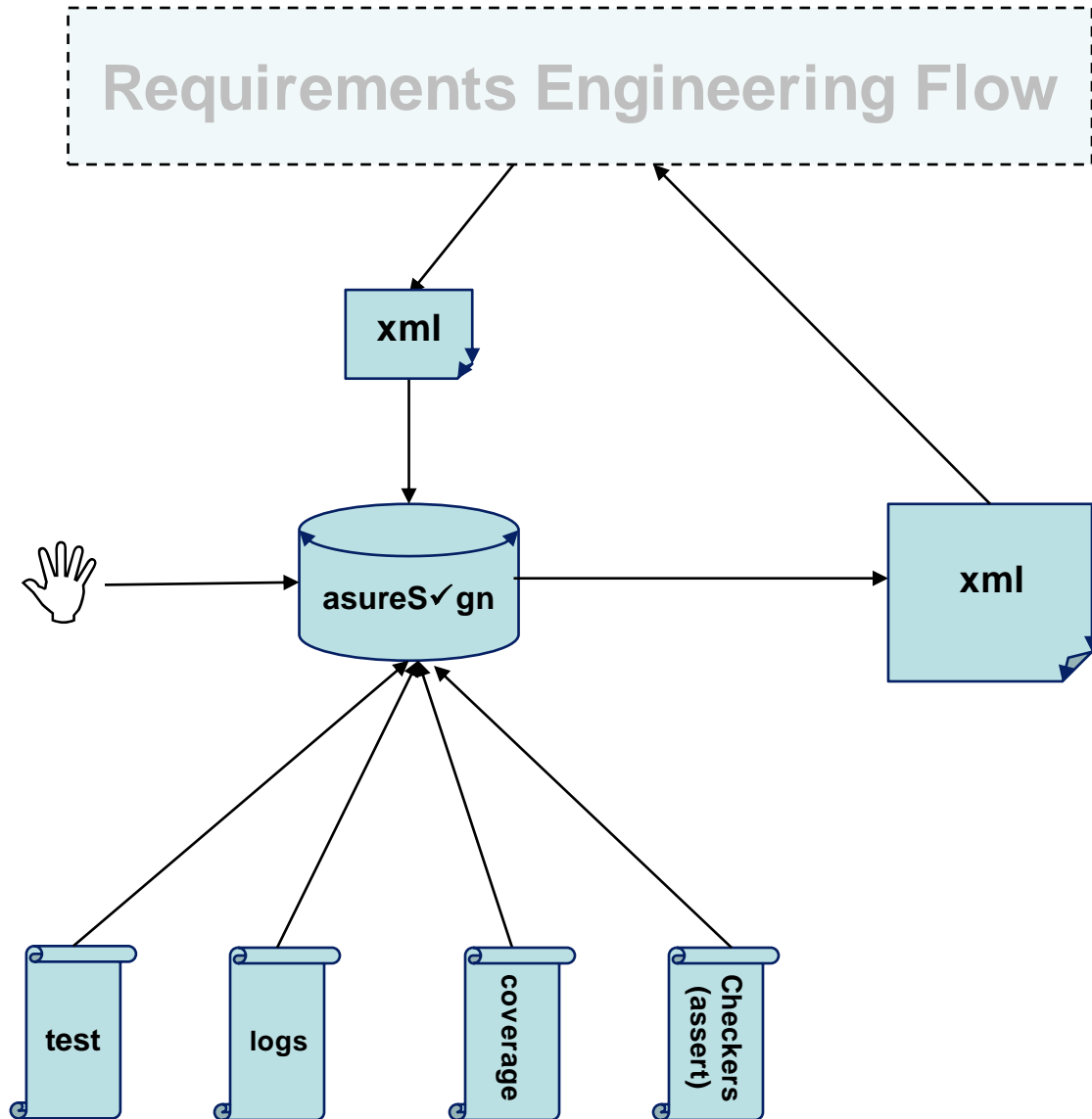
CHALLENGES

- Requirement interpretation may change through flow
- Manually mapping of documents with identifiers is time-consuming and subject to error
- Translation or moving of data may cause corruption or error
- Link to proofs of implementation/results is manual
- Visibility of Requirements through the entire tree is complex
- Communication across domains (pre-silicon/post-silicon) complex

Under Verification:

- Requirements not implemented
 - Incorrect testing due to miscomprehension
 - Re-spin due to late realisation
- Over Verification:
 - Resource cost
 - Duplication of effort
 - Incorrect product (size/speed etc)

TIGHTLY INTEGRATED RE & TEST



Allows Requirements driven Verification methodology

Requirements can be imported from external tool: 'top-level test plan'

Requirements can be refined and matched to goals: 'bottom-level test plan'

Mapping of the Requirements to test plan and results

Accumulates data over a period of time

- **Analyses and presents the status of tests**
- **Collects and presents coverage metrics**

Works across multiple test types (random, formal, directed, manual, assertions etc)

Control of pass/fail criteria on a per milestone/per group level

Allows easy control and evaluation of the progress of the project.

MAPPING GOALS TO COVERAGE OR TESTS

Editor Tools Help

Locking Status: Node is unlocked.

Filter Text: Search

Item	Kind	%	Implemented	De
internalTest	ARCH	26.83	11	
SPI Master	ARCH	71.43	10	
Write and Read	ARCH	75.00	3	
Write-only	ARCH	66.67	2	
Write and Read	ARCH	0.00	0	
7Bit Addr	DirectedTest	100.00	1	
10Bit Addr	DirectedTest	100.00	1	
Master	DirectedTest	100.00	1	
Hardware	IMPL	100.00	7	
Clock Formats	ARCH	100.00	6	
Simple Transmit Receive	IMPL	100.00	2	
Single Slave Select	IMPL	100.00	2	
Multiple Chained Slaves	DirectedTest	100.00	1	
1 Slave Passive, 1 Active	DirectedTest	100.00	1	
Frequency Operation	DirectedTest	100.00	1	
Software	IMPL	0.00	0	

Details for Verification Goal 'Master'

Goal Kind: Statement

Signed Off: Obsolete: Manual Signed Off:

Design Type: Instance Module None

Goal Name: Master

Mapping String: *bitwaitstate_test*

Parameters:

Item Name:

User: gaurav Required %age: 100

Specification:

Mapped metrics Unmapped metrics All metrics

Tests Functional Structural Assertions

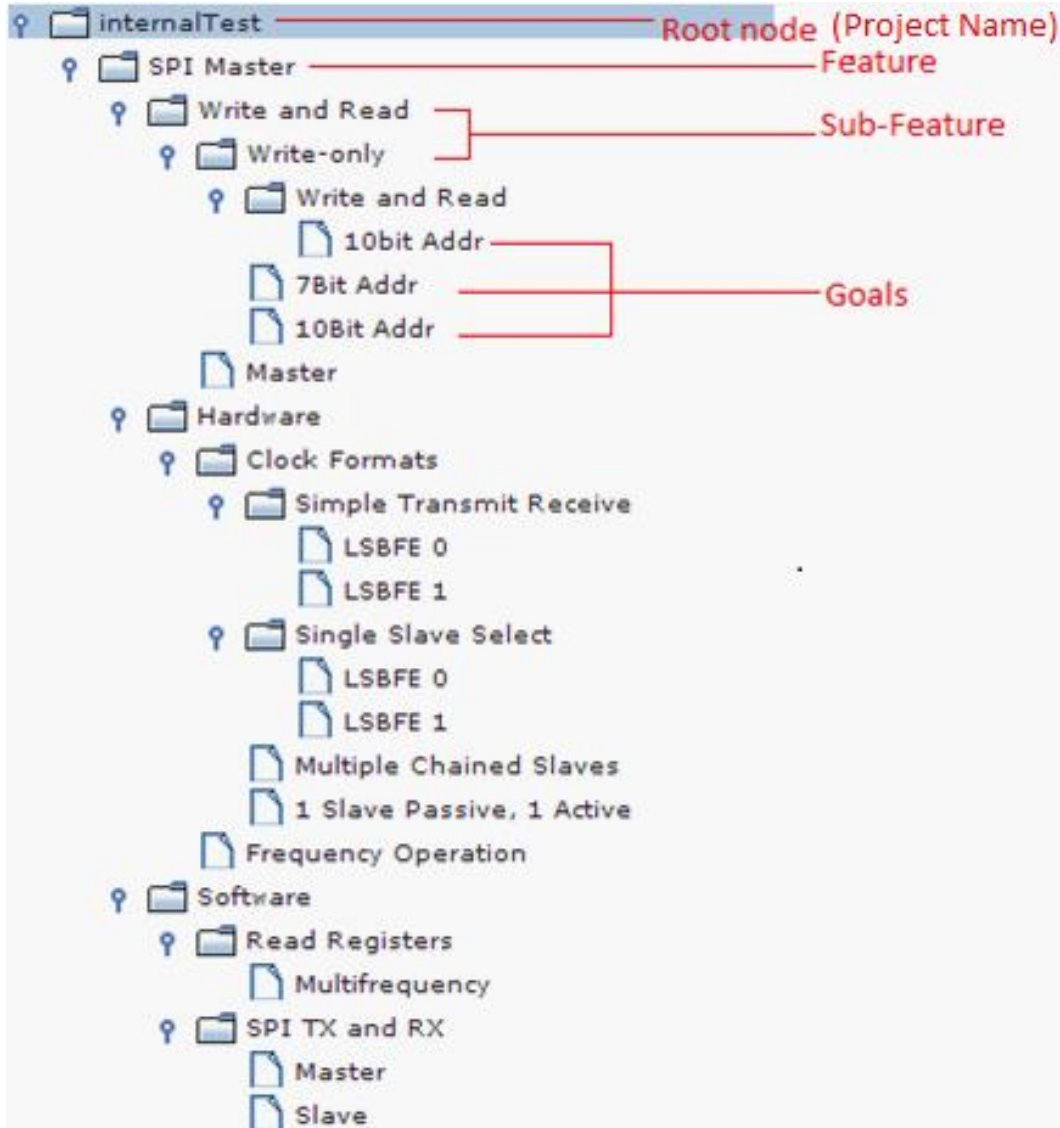
DirectedTest

Page: 1 of 1 First <<Prev Next>> Last

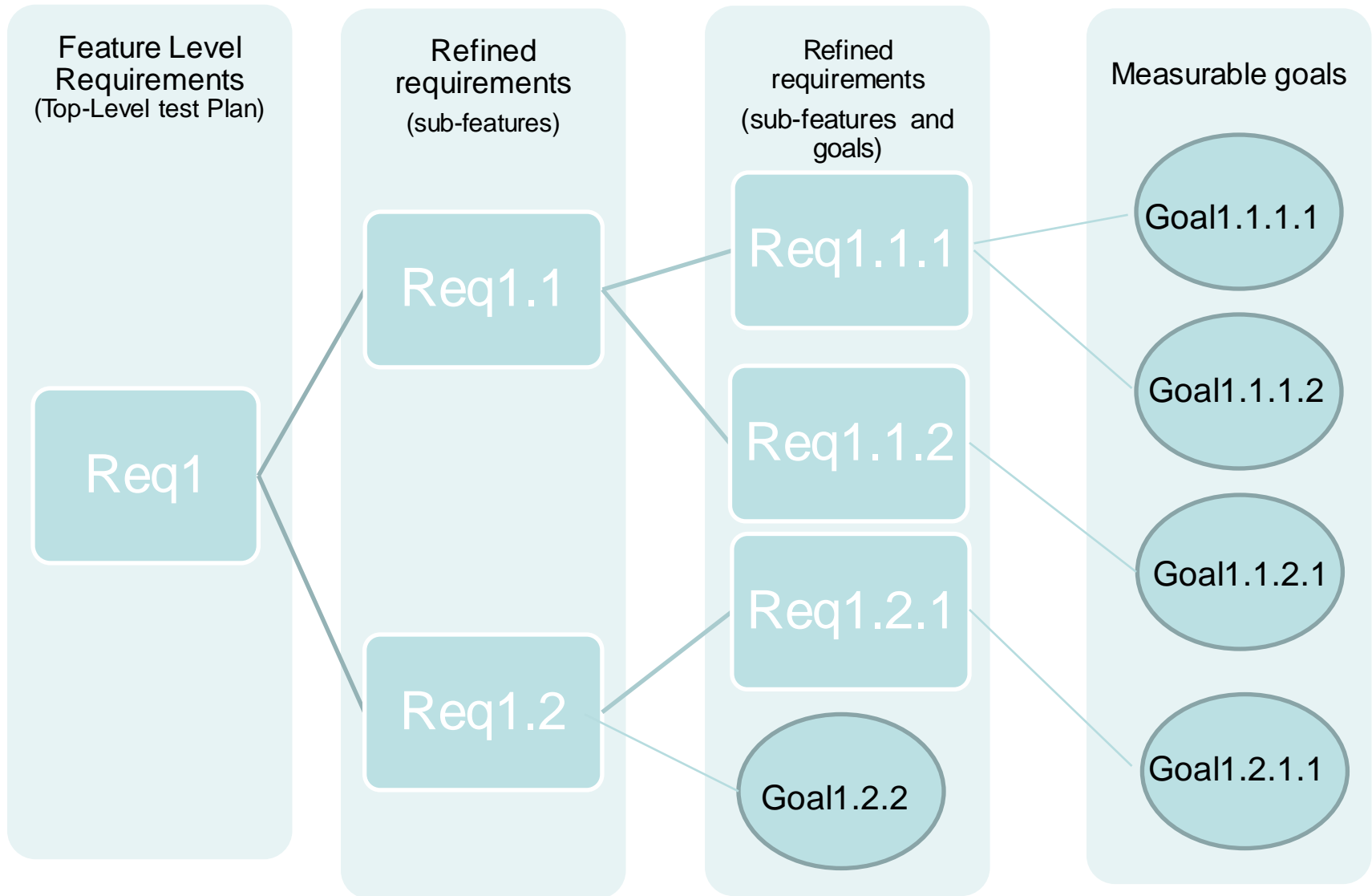
Test_Name	Parameter	User
no_test		no_user
tv_sio_i2c/sv/tvs_sio_i2c_mst_rtl_10slv1_10slv2_wr_8bit_data_norm...		luis
tv_sio_i2c/sv/tvs_sio_i2c_mst_rtl_7slv1_10slv2_wr_8bit_data_hs_mo...		nargis
tv_sio_i2c/sv/tvs_sio_i2c_mst_rtl_7slv1_10slv2_wr_8bit_data_hs_mo...		luis
tv_sio_i2c/sv/tvs_sio_i2c_mst_rtl_7slv1_10slv2_wr_8bit_data_norm...		raghu
tv_sio_i2c/sv/tvs_sio_i2c_mst_rtl_7slv1_10slv2_wr_8bit_data_norm...		mike
tv_sio_i2c/sv/tvs_sio_i2c_mst_rtl_7slv1_active_10slv2_passive_wr_8...		nargis
tv_sio_i2c/sv/tvs_sio_i2c_mst_rtl_single_slv_bfm_wr_10addr_8bit_us...		nigel
tv_sio_i2c/sv/tvs_sio_i2c_mst_rtl_single_slv_bfm_wr_10addr_8bit_us...		simon
tv_sio_i2c/sv/tvs_sio_i2c_mst_rtl_single_slv_bfm_wr_10bit_addr_8bi...		mike
tv_sio_i2c/sv/tvs_sio_i2c_mst_rtl_single_slv_bfm_wr_10bit_addr_8bi...		nigel
tv_sio_i2c/sv/tvs_sio_i2c_mst_rtl_single_slv_bfm_wr_7addr_8bit use...		nigel
tv_sio_i2c/sv/tvs_sio_i2c_mst_rtl_single_slv_bfm_wr_7addr_8bit use...		raghu

Showing 66 of 66

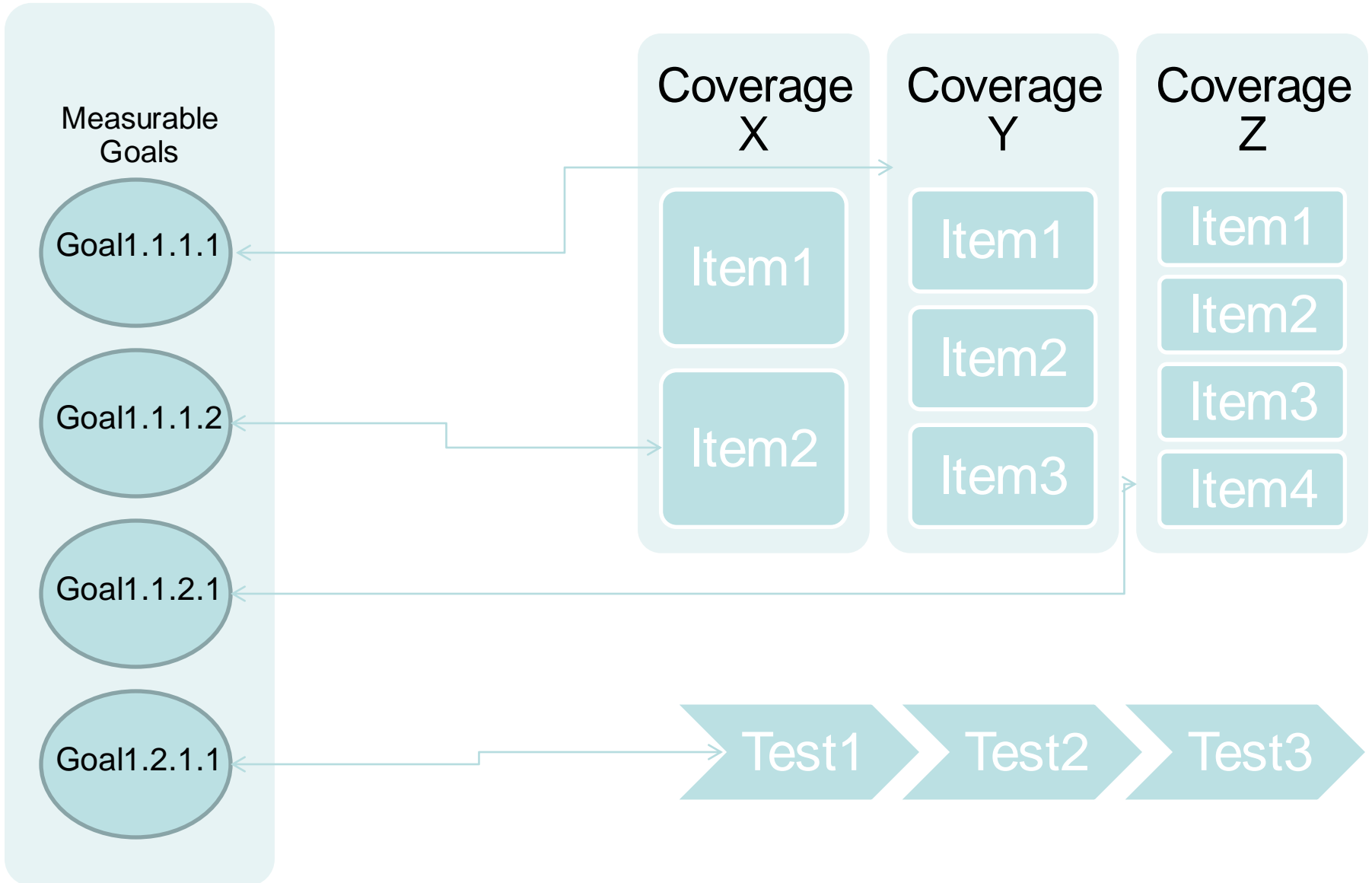
COMPLIANCE : HIERARCHICAL SET OF REQUIREMENTS



REFINING THE REQUIREMENTS TO TEST DESCRIPTION LEVEL



MAPPING GOALS TO COVERAGE OR TESTS



MAPPING GOALS TO COVERAGE OR TESTS

- Each goal can be mapped to one or more metrics (and each metric to one or many goals)
- During the lifecycle of the project goals relating to milestones may change their percentage coverage required for a pass
- Assigning milestones to goals allows management of early releases, easily identifies maturity of project and identifies resource or time risks

- Unmapped goals = test plan with no test.
 - New test/metric required.
- Unmapped metric = test but no plan or requirements.
 - Implicit or explicit requirement missing for requirements list (completeness)
 - Test/metric no longer needed – saves maintenance
- Obsolete features and goals identify variant differences
 - Don't run those mapped metrics/tests for this variant (saves regression size/runs and debug)

CONFIGURATION MANAGEMENT

asureS✓gn™ captures all the metrics and test data based on a unique Regression.

asureS✓gn™ can generate a unique identifier for a regression based on:

- A Version Control System
- A Time Stamp

Version Control System (VCS):

Regressions can be generated based on the state of VCS. This identifies the version (config/label/tag) of the code against which the tests were run and can also track the changes between two versions of source code.

Supported version control systems are:

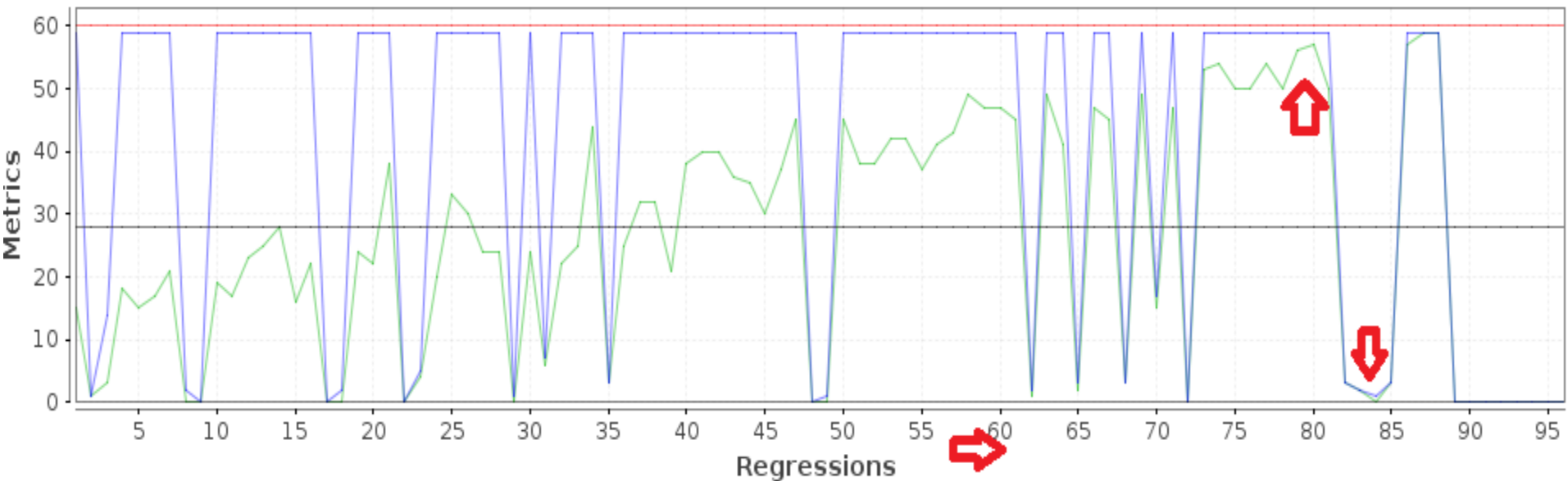
- Git
- SVN
- Clearcase

Timestamp: Regressions can also be generated based on the current timestamp. This is helpful if there is no VCS or the user doesn't wish to link the results to any VCS version.

1. Proper verification steps are always executed with each regression.
2. Verification is performed strictly on the basis of Requirements, thus both Over verification and Under verification are properly handled.
3. Project progress graph and milestones are the best indicator of how project is progressing, and both Engineers and Managers can benefit from it.
4. Release dates can be properly identified.
5. Efforts can be closely associated with Requirements.

PROJECT HISTORY GRAPH

- Is a key indicator of the overall progress of the project.
- Any dip or peaks indicate debugging and corrective actions may be required.
- Graph can be plotted [Metrics vs Regression or Date]



CONFIGURATION MANAGEMENT ASSISTS DEBUG

Regression Details

Description: git path
Started At: Thu Apr 03 18:06:37 IST 2014

Page : 1 of 1 First <<Prev Next>> Last

Name	Type	Version
gitrepo2	git	71da0eefb33175704a47251f8e0...

filter filter filter

| Showing 1 of 1

Modified Files

- git|gitrepo2: M .gitignore
- git|gitrepo2: M .idea/ant.xml
- git|gitrepo2: M .idea/compiler.xml
- git|gitrepo2: M .idea/runConfigurations/Dashboard.xml
- git|gitrepo2: M .idea/runConfigurations/UpdateGraphData.xml
- git|gitrepo2: M Documentation/html/CommandLineUtils.html
- git|gitrepo2: M Documentation/html/Components.html
- git|gitrepo2: M Documentation/html/FAQ.html
- git|gitrepo2: M Documentation/html/Index.html
- git|gitrepo2: M Documentation/html/Installation.html
- git|gitrepo2: M Documentation/html/Overview.html
- git|gitrepo2: M Documentation/html/PerAPIExample.html
- git|gitrepo2: M Documentation/html/Release_Notes.html
- git|gitrepo2: M Documentation/html/Usage.html
- git|gitrepo2: M Documentation/html/User.html
- git|gitrepo2: M Documentation/html/XMLImportExample.html
- git|gitrepo2: M Documentation/html/XMLImportXSD.html
- git|gitrepo2: M Documentation/html/assign.html
- git|gitrepo2: M Documentation/html/layout-as.css
- git|gitrepo2: M Documentation/html/runGui.html
- git|gitrepo2: M Documentation/html/runStartRegression.html
- git|gitrepo2: M Documentation/html/runTestBegin.html
- git|gitrepo2: M Documentation/html/runTestEnd.html
- git|gitrepo2: M Documentation/html/runUcdbReader.html
- git|gitrepo2: M Documentation/html/runUpdateDashboardData.html

OK

For an observable change in the graph, the Regression Details window is available to identify what source code has changed. This may help quickly identify a source of the change.

REQUIREMENTS HIERARCHY

- A pass criteria can be assigned by milestone, project, feature, sub-feature or goal
- Pass criteria may be related to the importance of test (Safety level)
- Keeping the hierarchy within one tool simplifies Requirements Traceability

Item	Kind	%	Passed	Total	Uid
📁 Demo	ARCH	99.54	5,881	5,908	1
📁 RfQ00_Assertion	ARCH	93.90	154	164	4
📄 assert basic demand access	Aggregat...	93.90	77	82	7
📄 assert Read Boot VOD	Aggregat...	93.90	77	82	8
📁 RfQ00_Functional	ARCH	99.95	5,715	5,718	5
📁 Bus Interface	ARCH	66.67	6	9	11
📄 Check TCK clock off in	CoverBin	50.00	3	6	12
📄 Check frequency range f	CoverPoint	100.00	3	3	13
📄 Check_MTag_not_tested	CoverBin	0.00	0	0	17
📄 Check_Master_Tag	CoverPoint	100.00	3	3	9
📄 Check SVM and ENDINIT	CoverPoint	100.00	5,704	5,704	10
📄 Manual_check_master_tag	CoverPoint	100.00	1	1	18
📄 Manual_check_SVM	CoverPoint	100.00	1	1	19
📁 RfQ00_Structural	ARCH	46.15	12	26	6
📁 RfQ00_Obs_req	ARCH	0.00	0	0	20
📄 OBS_req_Test	DirectedT...	0.00	0	0	21
📄 OBS cov test	CoverGroup	0.00	0	0	22

MILESTONES

Milestones are **user defined significant events** in the course of a project and are key indicator **to identify the maturity of the project**. Various milestones can be created e.g. alpha ready, beta ready etc.

For early releases from one group (sub-system -> system) this can assist with communication – features passing/failing at each milestone

Page : 1 of 1

UID	Hierarchy	Feature/Goal	Actual	Gold	Silver	Bronze	Sapphire	Emerald	Quartz
1		Demo	98.36	99.0	75.0	50.0	13.0	5.0	2.0
4	Demo/	Check_Assertion_Req	22.64	93.0	0.0	0.0	0.0	0.0	0.0
7	Demo/Check_Assertion_Req/	assert basic instance	29.27	93.0	0.0	0.0	0.0	0.0	0.0
8	Demo/Check_Assertion_Req/	assert basic Module	0.0	91.0	0.0	0.0	0.0	0.0	0.0
23	Demo/Check_Assertion_Req/	New Goal	0.0	93.0	0.0	0.0	0.0	0.0	0.0
5	Demo/	Check_Functional_Req	100.0	90.0	75.0	10.0	10.0	0.0	0.0
11	Demo/Check_Functional_Req/	Bus Interface	100.0	60.0	60.0	0.0	0.0	0.0	0.0
12	Demo/Check_Functional_Req/Bus Interface/	Check_TCK_clock_off_in_I...	100.0	0.0	0.0	0.0	0.0	0.0	0.0
13	Demo/Check_Functional_Req/Bus Interface/	Check frequency range for...	100.0	100.0	100.0	0.0	0.0	0.0	0.0
17	Demo/Check_Functional_Req/Bus Interface/	Check_MTag_not_tested	0.0	0.0	0.0	0.0	0.0	0.0	0.0
9	Demo/Check_Functional_Req/	Check_Master_Tag	100.0	100.0	100.0	0.0	0.0	0.0	0.0
10	Demo/Check_Functional_Req/	Check_SVM_and_ENDINIT	100.0	100.0	75.0	9.0	8.0	8.0	0.0
18	Demo/Check_Functional_Req/	Manual_check_master_tag	100.0	100.0	0.0	0.0	0.0	0.0	0.0
19	Demo/Check_Functional_Req/	Manual_check_SVM	100.0	100.0	0.0	0.0	0.0	0.0	0.0
6	Demo/	Check_Structural_Req	46.15	45.0	0.0	0.0	0.0	0.0	0.0
20	Demo/Check_Structural_Req/	Obsolete_Req	0.0	0.0	0.0	0.0	0.0	0.0	0.0
21	Demo/Check_Structural_Req/Obsolete_Req/	OBS_req_Test	0.0	0.0	0.0	0.0	0.0	0.0	0.0
22	Demo/Check_Structural_Req/Obsolete_Req/	OBS_cov_test	0.0	0.0	0.0	0.0	0.0	0.0	0.0
14	Demo/Check_Structural_Req/	Check_Statement_coverage	41.67	40.0	0.0	0.0	0.0	0.0	0.0
15	Demo/Check_Structural_Req/	Check_Brnach_coverage	100.0	100.0	0.0	0.0	0.0	0.0	0.0
16	Demo/Check_Structural_Req/	Check_Aggr_Branch_cover...	100.0	100.0	0.0	0.0	0.0	0.0	0.0

filter filter filter filter filter filter filter filter filter filter

REGRESSION COMPARISON

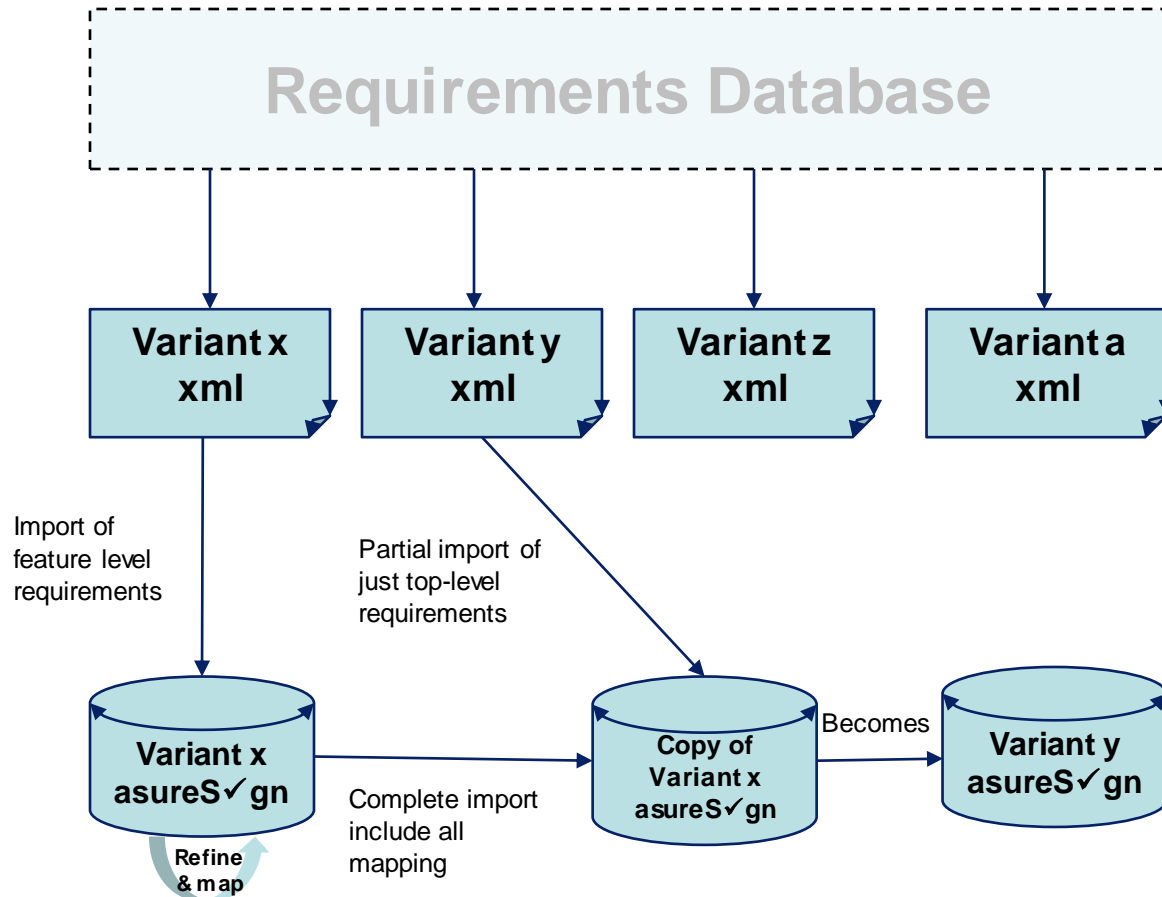
Regression comparison helps debug and identify differences over time

Regression Compare and Metric/Goal Debug							
Debug: Metric View							
DETAILS		REGRESSION 6		REGRESSION 7		REGRESSION 8	
PASS		4638/21292		6276/21292		19446/21292	
FAIL		1860/21292		0/21292		870/21292	
METRIC MISSING		2246/21292		2988/21292		976/21292	
NEW METRIC		0/21292		0/21292		0/21292	
Page : 1 of 213 First <<Prev Next>> Last							
Metric Type	Metric Item	Regression 6		Regression 7		Regression 8	
		STATE	GOAL	STATE	GOAL	STATE	GOAL
DirectedT...	/mod02/xxx0007/BOOT_OPTIONS	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx0007/xxx0008_xxx0009_xxx0010	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx0007/xxx0011_xxx0012_xxx0013	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx0007/xxx0011_xxx0012_xxx0014	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx0007/xxx0011_xxx0012_xxx0015	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx0007/xxx0011_xxx0012_xxx0016	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx2779/BOOT_OPTIONS	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx2779/xxx0008_xxx0821	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx2779/xxx0008_xxx0821_xxx0360	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx2779/xxx2780_xxx0821	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx2779/xxx2780_xxx0821_xxx0360	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx2779/xxx2781_xxx0821	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx2779/xxx2781_xxx0821_xxx0360	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx2779/xxx2782_xxx0821	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx2779/xxx2782_xxx0821_xxx0360	PASS	1	METRIC_...	1	PASS	1
DirectedT...	/mod02/xxx2779/xxx0011_xxx0821_xxx2783	PASS	1	METRIC_...	1	PASS	1
COVERGR...	/top/F30/mod01/xxx0001/xxx0002/xxx0003	METRIC_...	UNMAPPED	METRIC_...	UNMAPPED	PASS(1/1)	UNMAPPED
COVERPO...	/top/F30/m...01/xxx0001/xxx0002/xxx0003/tag	METRIC_...	1	METRIC_...	1	PASS(1/1)	1
coverbin	/top/F30/m...01/xxx0001/xxx0002/xxx0003/tag	METRIC_...	1	METRIC_...	1	PASS(1/1)	1
COVERGR...	/top/F30/mod01/xxx0001/xxx0002/xxx0010	METRIC_...	UNMAPPED	METRIC_...	UNMAPPED	PASS(1/1)	UNMAPPED
COVERPO...	/top/F30/m...01/xxx0001/xxx0002/xxx0010/tag	METRIC_...	1	METRIC_...	1	PASS(1/1)	1
coverbin	/top/F30/m...01/xxx0001/xxx0002/xxx0010/tag	METRIC_...	1	METRIC_...	1	PASS(1/1)	1
COVERGR...	/top/F30/mod01/xxx0001/xxx0002/xxx0012	METRIC_...	UNMAPPED	METRIC_...	UNMAPPED	PASS(6/6)	UNMAPPED
filter	filter	filter	filter	filter	filter	filter	filter

OTHER FEATURES

- Multiple user access.
- Supports UCIS standard.
- Supports locking of requirements for protection.
- Tailored Report generation for audit, with description for goals(test plan within the tool and easily updated)
- Supports batch and bulk operations.
- XML support allows easy integration with other tooling.
- Features and goals may be edited, manipulated and enhanced inside the tool.
- Internal comments allowed to help communication within a project
- Requirements can be signed-off manually – if by manual inspection e.g waveform
- Coverage Exclusion.

Variant Management



Upcoming enhancements:

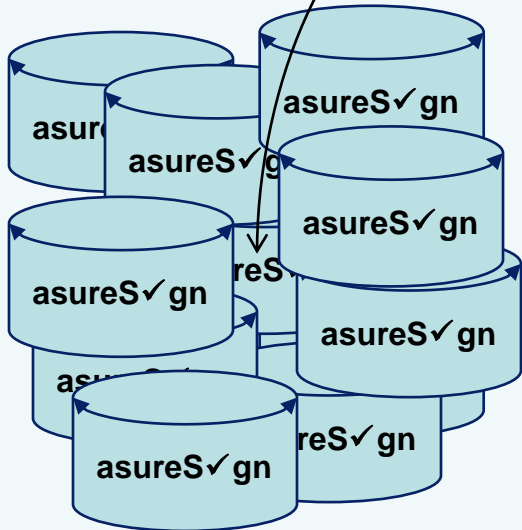
- Web based Interface, with configurable Dashboard.
- Complete support for 64 bit machines.
- Better support for multiple vendors to capture Coverage.
- Improved capability to capture Requirements from different formats.
- API support to capture and generate additional reports.
- Observation coverage.
- Improved support for Windows.
- Etc...

Domain Analyser Dashboard

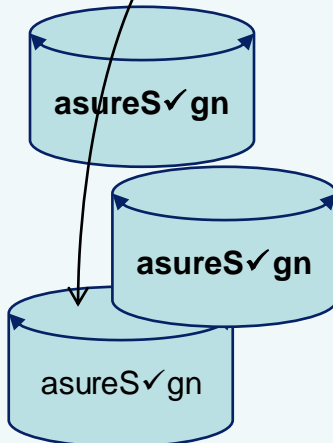
Req	Pre-silicon IP	Pre-silicon SOC	Validation IP	Validation SOC
Req_x	pass	No	fail	No
Req_y	no	pass	No	pass

API Interface

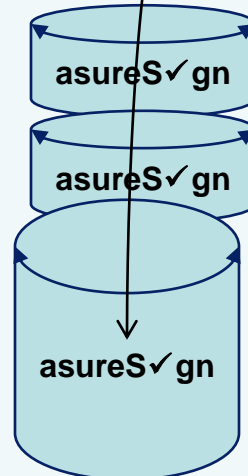
Pre-silicon IP



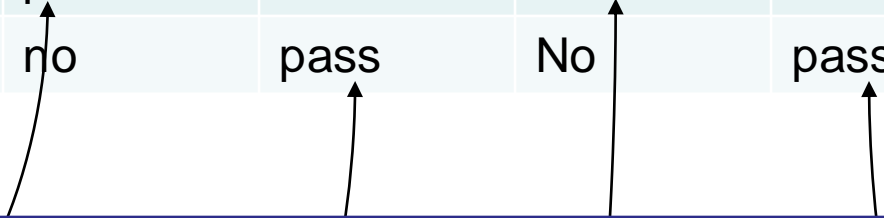
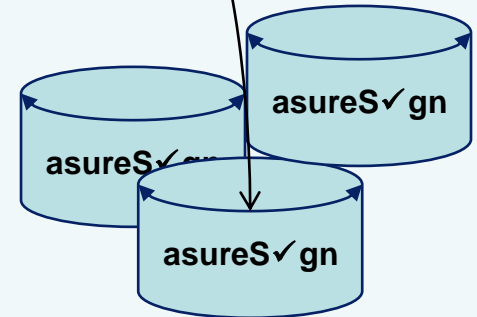
Pre-silicon SOC



Validation IP



Validation SOC, Firmware, software etc



- **Same as Dashboard but for quick verification analysis**
 - All History Graphs
 - All History Tables
 - Change management issues
 - Coverage overview per 'Goal' (test requirement)
- **Replaces in-depth weekly reports**

CONTACT:

THANK YOU

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T&VS <http://testandverification.com/>