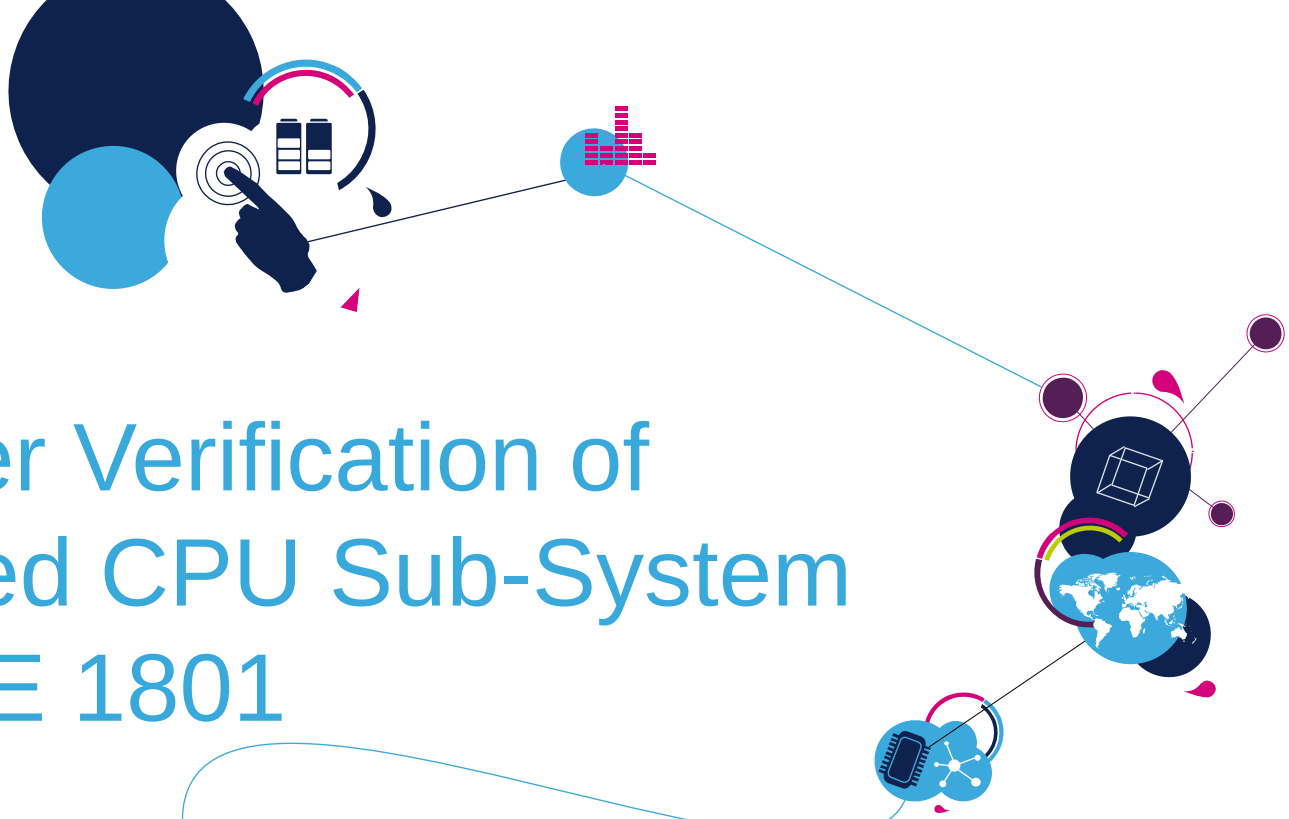

Low Power Verification of ARM based CPU Sub-System using IEEE 1801

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Verification Future Conference, Bangalore

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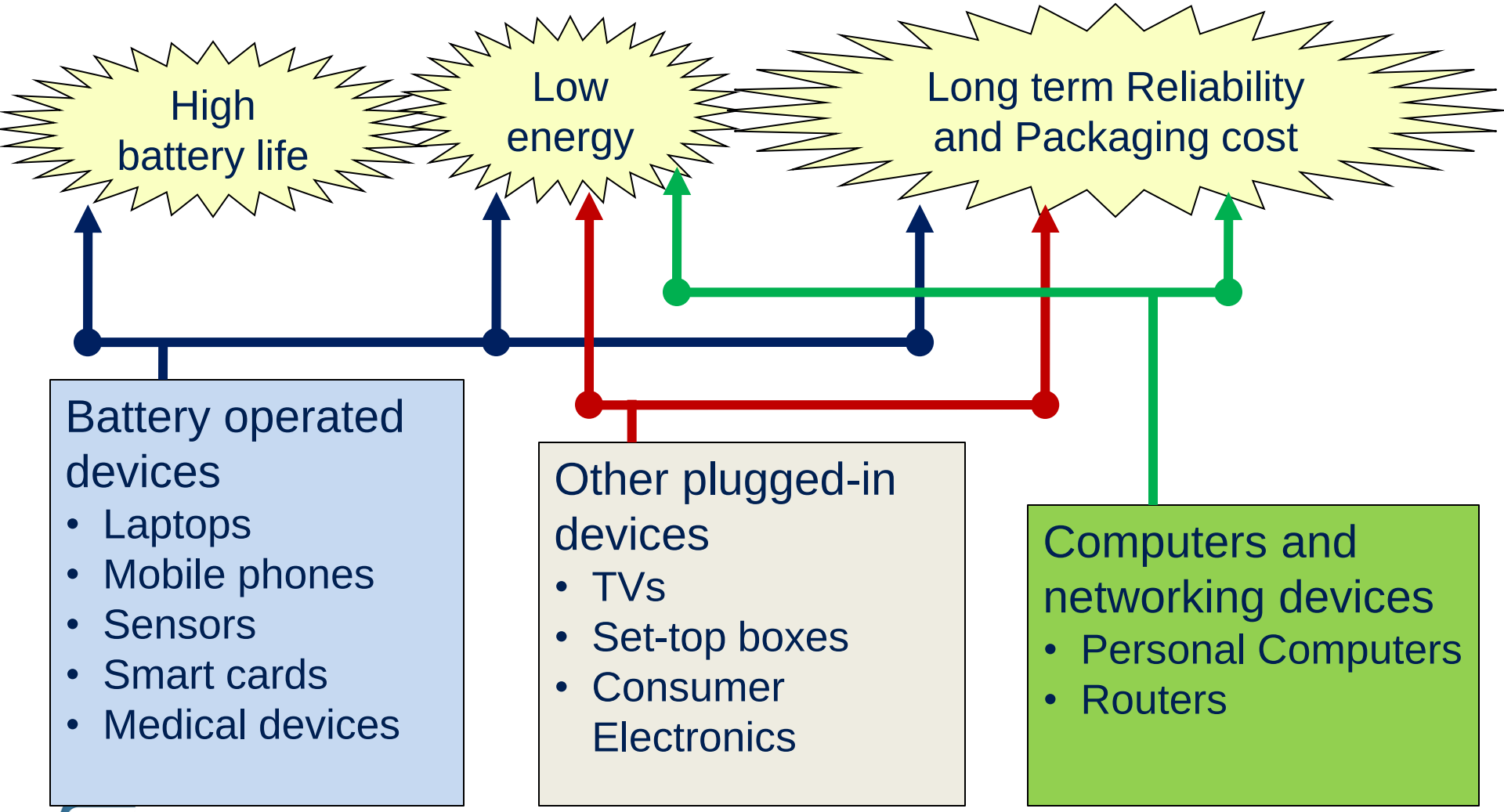
life.augmented

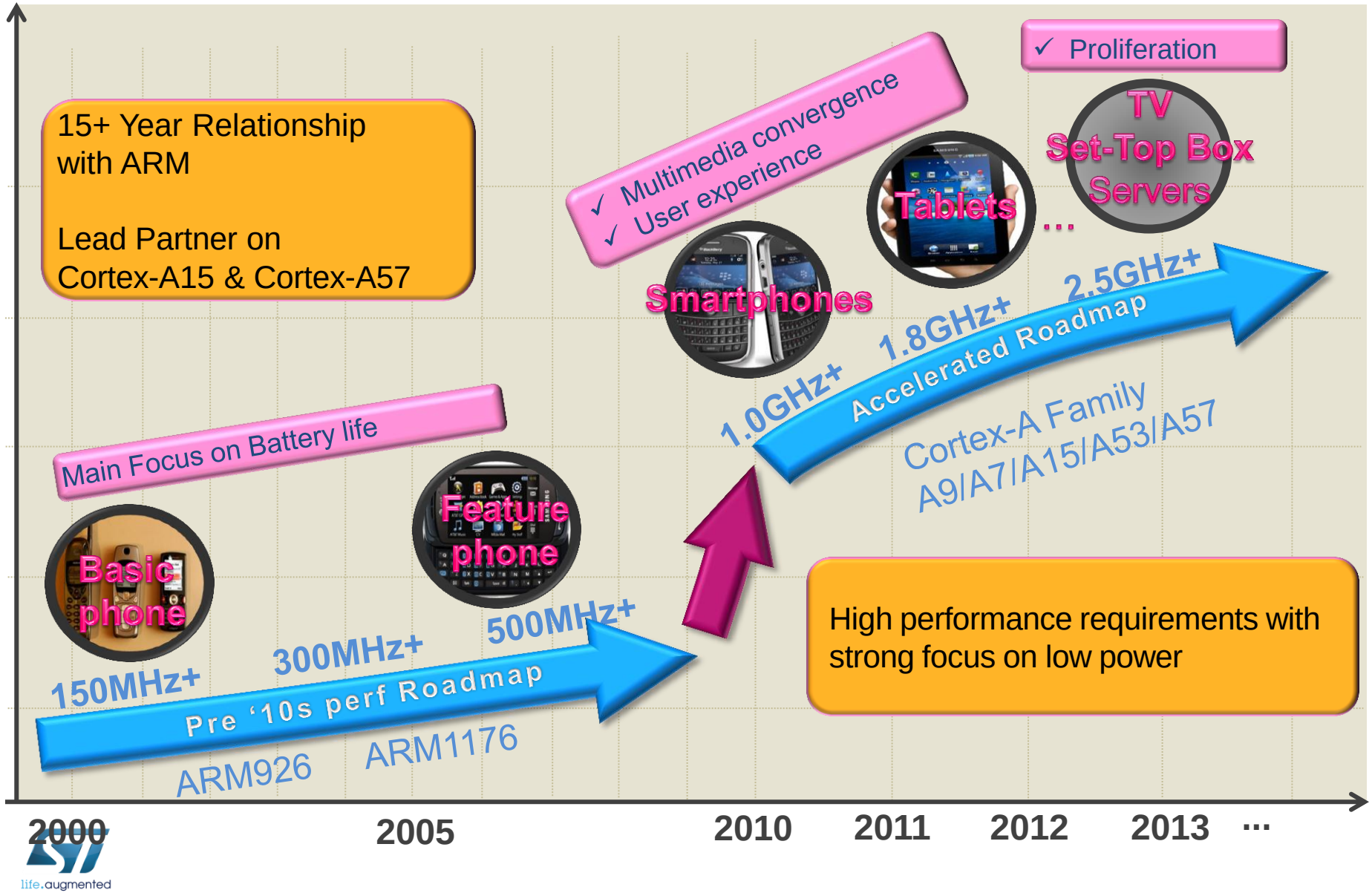
Agenda

- Need for low power devices
- Power architecture - ARM cores based ST CPU Sub-System
- Low power verification challenges
- Use cases
- Summary

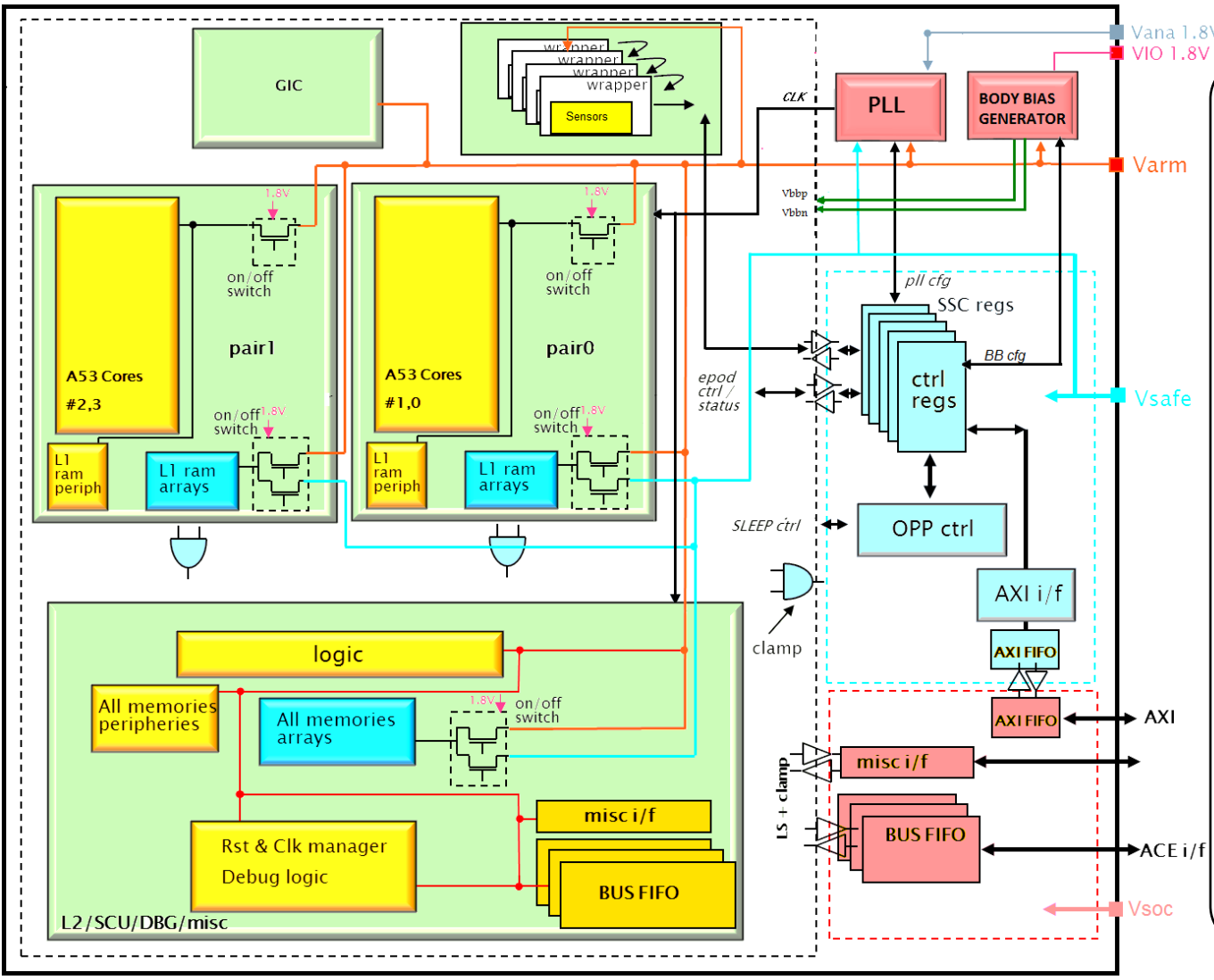
Low Power is Becoming Pervasive…



ARM Core Usage A Long History at ST

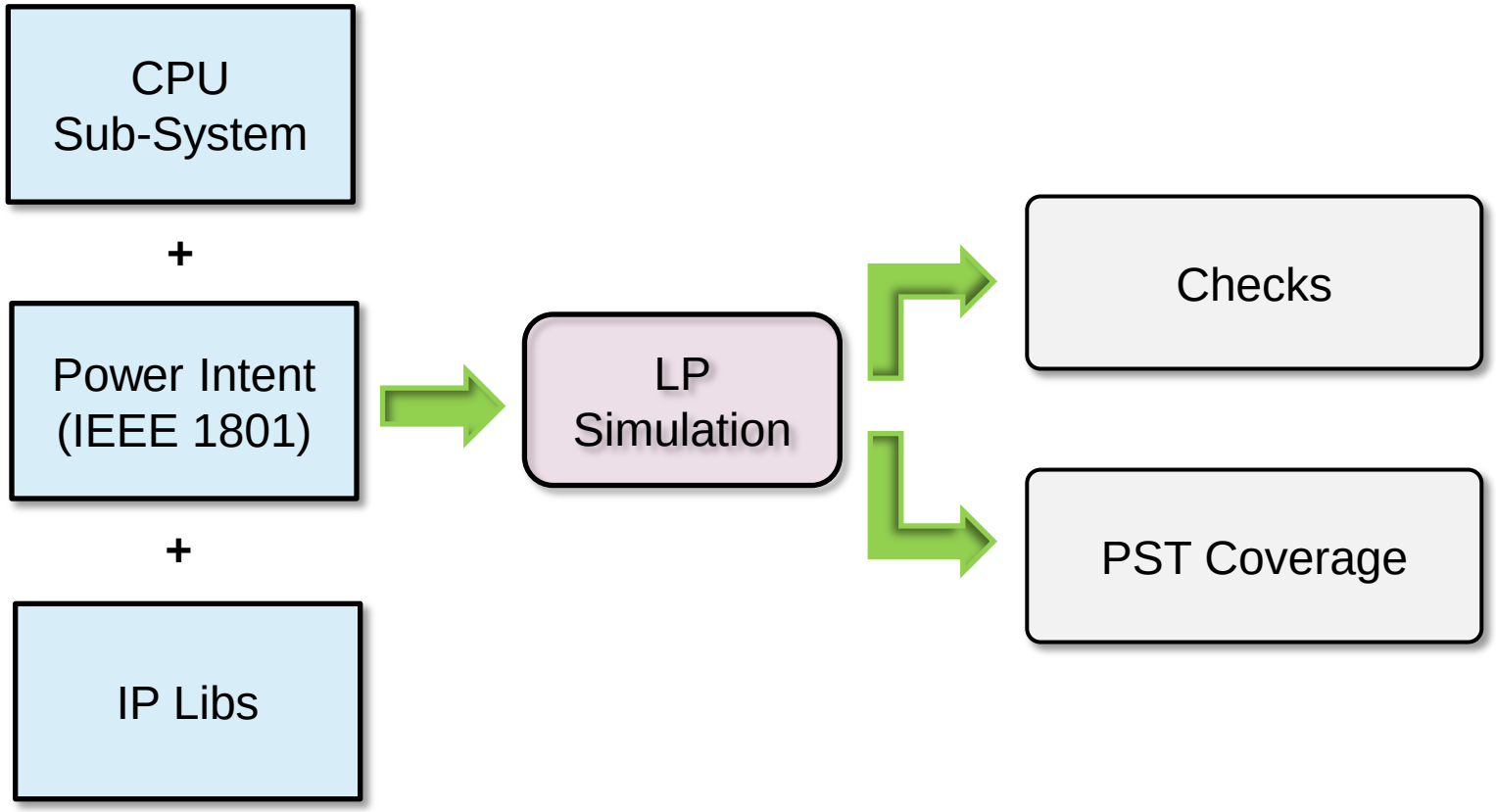


Advance low Power in CPU Sub-System

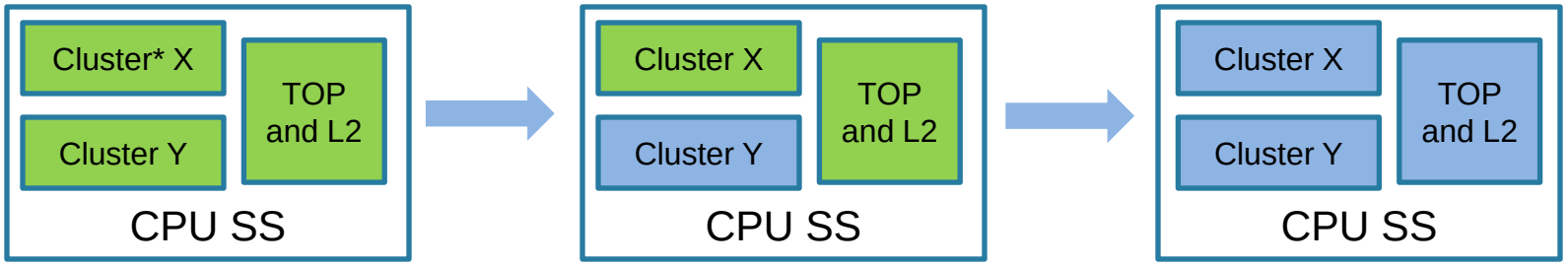


- Dynamic Voltage and Frequency Scaling
  - Multi Voltage Domains
  - Level Shifters
  - Sensors & Power Controllers
- Partial shutdown
  - Multi Power Domains
  - Power Switches
  - Isolation Cells
- Retention
  - Multi-rail Memories
- Body Biasing
  - Body Bias IPs
  - Bias Voltage Connects

Low Power Verification Flow



Power Sequence Verification



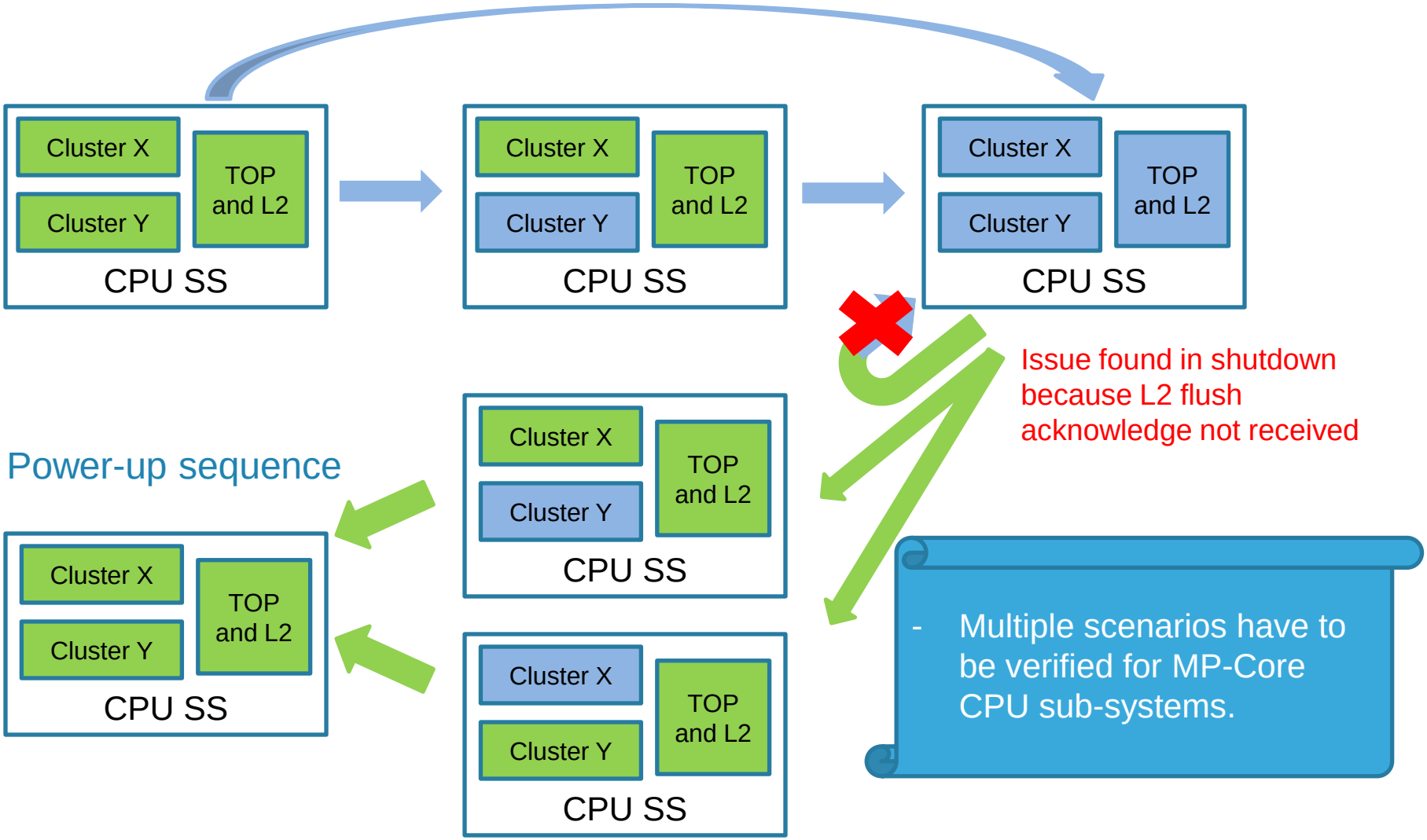
Shut-down Sequence

- Flush cluster X pipeline, wait for acknowledge
- Flush cluster X L1 cache , wait for acknowledge
- Clamp cluster X outputs
- Shutdown cluster X
- Shutdown cluster Y, similar to cluster X
- Flush L2 cache, wait for acknowledge
- Clamp outputs
- Power down the L2 sub-system

*Cluster consists of multiple CPU cores

ON
OFF

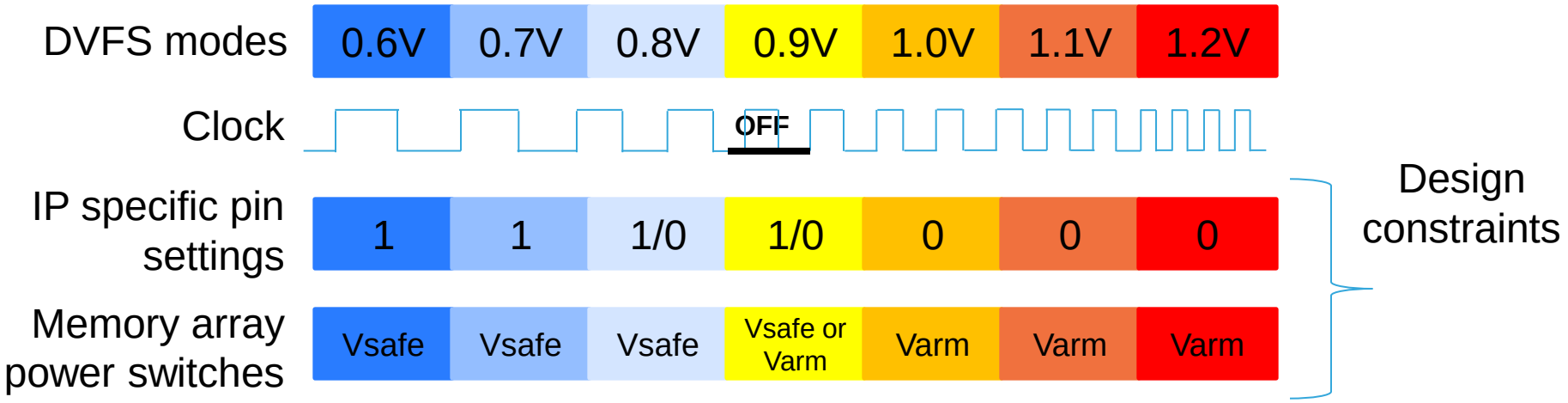
Power Sequence Verification



*Cluster consists of multiple CPU cores

ON
OFF

DVFS Verification



- Verification of the above constraints at each operational point (OPP) is critical
- Transition between various OPP points
  - Intermediate states
  - Internal control sequence
- Body bias states (FBB, RBB, etc.)
  - Body voltages may be generated by on-chip generators involving dedicated controllers , which poses additional verification complexity

Summary

- Advance low power techniques are essential for meeting CPU performance targets
- Implementation involves augmenting RTL design with power management IPs and defining power intent through IEEE-1801 UPF
- Combination of power sequences, extreme DVFS and other low power techniques like body biasing, retention, etc. poses challenge in low power verification of multi-core CPU sub-systems
- Low power features have added a new dimension to design verification requiring specialized methodologies and tools

Thank you