Verification Challenges - An FPGA perspective

Andy Walton,
Senior Member of Technical Staff
Systems Solution Engineering, Networking.

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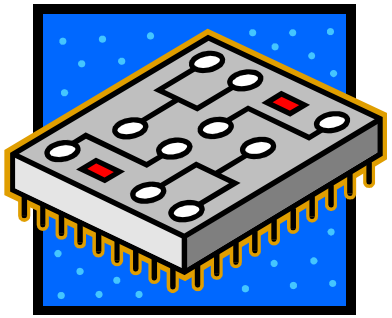
Why these challenges?

- **Wanted to focus on challenges that are more relevant to FPGA designs**
  - Others have focused on “cross-platform” challenges.
    - We have those too…
- **Designs considered are mainly “traditional”**
  - RTL design
  - Re-use from previous project
    - Usually with some modification
  - Use of “standard” IP
  - Incorporates 3rd-party RTL



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Working with the FPGA USP – flexibility

- **FPGAs have the flexibility of software**
  - Can iterate the design, provide updates, experiment, etc.
- **Creates expectation of software-like attributes**
  - Start development whilst requirements still “in-flux”
    - Late changes are not a “surprise”
  - “Agile” approach to development – small changes/additions to working design
  - Move functionality between versions, releases, etc.
  - Lower-bar for “release quality” (at least before moving to lab)
- **FPGAs are still hardware though…**
  - Not so easy to debug, still need to close timing, etc.
- **“Waterfall” approach to verification doesn’t work**
  - No large “up front” time to develop complex environment
  - Can’t keep having large non-productive periods whilst environment updated

Need a more Agile/rapid-proto-typing approach to verification

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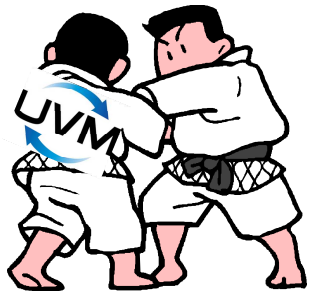
When the system-level verification environment is UVM …but the block-level isn't…and sometimes when it is!

- **Designs use IP/sub-systems from various sources**
  - Previous projects, other groups, customers, etc.
- **Usually not supplied with UVM environment**
  - Makes end-to-end checking difficult
    - May need to write new scoreboard/reference models from scratch
  - Need to re-create any configuration stimulus, transactions, etc.
  - Can be a barrier to adopting UVM



Need interworking between "legacy" and UVM world.

- **When UVM environments are provided, don't always "play nicely" together…**
  - Can *usually* use in "passive" mode for checking
    - …as long as all register-based scoreboard configuration is done via monitors
  - Stimulus (eg. configuration) not always so easy to reuse

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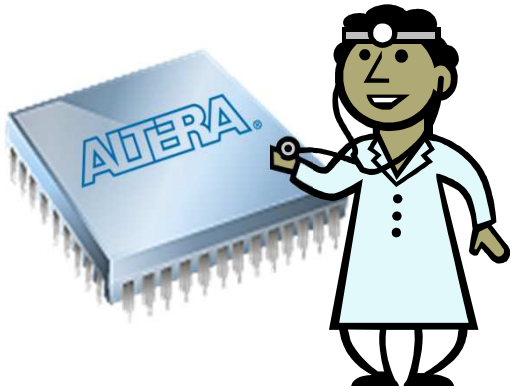
"But we can just run it on the hardware" …and sometimes they're right!

- **Difficult to justify "holding back" on hardware:**
  - You'd never ask a s/w engineer to use an ISS when a CPU was available!
  - Productivity is far higher due to speed…at least when everything is working
  - Management pressure to "get on the hardware"



- **BUT**
  - Final hardware not always available
    - May have to use "demo boards" without full functionality
  - Very difficult to debug complex problems
    - FPGA designs are larger than ASICs were a few years ago!
  - Can't easily transfer information back to simulation environment for debug
  - Can't be sure what's *really* been tested (no hardware coverage)

Need some unified methodology/tools to unify h/w ↔ simulator environments

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Verification of designs which use partial reconfiguration.

- **Partial reconfiguration allows elements of FPGA to be re-used**
  - Loading done during runtime, possibly multiple times
  - Need to emulate “re-elaboration” during simulation
  - Similar to power-aware verification…but different.

How can we verify that the design operates correctly when the various sub-systems are loaded (or not present at all)?

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The ones that escaped…

- **We also considered…**
  - Finding suitably skilled verification engineers
  - The UVM methodology is
    - Too complex for many engineers to understand/use
      - More complex than the design!
    - Too simple to construct complex test-benches
      - A lot of user-code required
    - Too slow to compete with h/w engineers “privacy of their cubicle” test-benches
  - Verification of parameterised IP.

But many of these were covered last year…

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Thank You

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