Welcome to Verification Futures

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Verification Challenges

Dr Mike Bartley
CEO & Founder
Test and Verification Solutions Ltd

India 2013

Sainath Karlapalem, NXP	AMS Verification	Dynamic Power Verif	Timing Verification
Udaya Kumar Napa, MaxLinear	Coverage Closure	Integrating Levels of Verif	Requirements driven verification
Desikan Srinivasan, ARM	Exploiting Formal	System level coherency	Verif Schedule Predictability

Europe 2013

Chris Brown (Verification Manager), Broadcom, UK	Improved EDA competition through standardisation	Integration Testing: Improving IP to SoC verification reuse	
Simon Bewick (Director ASIC Development), Ericsson, UK	Measuring Testbench quality	Fewer bugs, earlier bugs	Verifying power intent
Andy Walton, Altera, UK	UVM @ system-level but not at block-level isn't	But we can just run it on the hardware	Verification of designs which use partial reconfiguration
Tim Joyce (Verification Manager), STMicro, UK	Predicting and finding verification resources	Functional Coverage at SoC level	SoC Simulation Complexity

France and Germany 2013

Jerome Bombal (Director SOC Verification), Samsung LSI, France	Sign-off integration verification plans	Verification SW libraries	Integration coverage toolboxes
Beatrice Brochier and Yassine Elkhourassani, STMicro	Verifying Interconnect at top level	Verifying IOMuxing in a complex SoC	
Martin Ruhwandl, Infineon Technologies	ISO 26262	Multi-site strategy/short term contractors	Analog-mixed signal engineers vs. digital engineers

Analysis for 2011 to 2013 (Top 9)

Complexity	7
Integrating Languages, Views and Techniques	7
Completeness	5
Productivity	5
Requirements Driven Verif (ISO 26262)	5
Scalability	4
Reuse	4
System	4
Mixed Signal	4

Analysis for 2011 to 2013

Complexity	7
Integrating Languages, Views and Techniques	7
Completeness	5
Productivity	5
Requirements Driven Verif/ISO 26262	5
Scalability	4
Reuse	4
System	4
Mixed Signal	4
HW/SW	3
Resources	3
Integration Verification	3
Design for Verif	2
Debug	2
Demonstrating Bug Absence	2
Synthesis/Timing Constraints	2
Power Verification	2
FPGA Specific	2
Performance	1
Change	1
Leading Edge Technology	1
Verification Data Mgt	1
Predictability	1
EDA tool Integration	1
Measuring Test Bench Quality	1
IO Muxing at SoC Level	1