3 Verification Challenges

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AMS Verification

- Pure AMS simulation->spectre
  - Longer Simulation run times
    - 5 days for one AMS test case compared to 1 hour Digital Mixed Simulation
      - Switching regulator simulation for 5 ms real time with APS(accelerated parallel simulator)
      - Highest Frequency module being WREAL model
  - Signal Probing
    - Huge disk space consumption (Compression ??)
    - Increased run-time
  - Controlling the input stimuli without affecting the restoration of existing design snapshot
    - Changing the voltage ramp-up behavior from 12v->15v from 12v->20v

- Digital Mixed Signal simulation-> WREAL models
  - What models have to be developed?
    - How to model realistic ramp up times of analog interfaces for accurate analog-digital interactions?
      - Capacitance effects
    - Automatic Model generation from Schematic??
  - Who and when models have to developed?
  - Formal equivalence check ->LVS kind of check between Model and Schematic?

Dynamic Power Verification

- Defining realistic use case scenario
- Developing use case for the simulation environment
  - Moving away from verification sw towards Application sw
  - Time consuming task.
    - Needs dedicated effort and attention
- Successful timing simulation run capturing real power and performance
- Early RTL simulation based dynamic analysis for power signoff???

	Requirement	Average Power (EPS with 10% activity)	Peak power(VCD based)	Silicon Measurement
Voltage/Freq.	1.2v/256MHz	1.2v/256MHz	1.2v/256MHz	1.2v/256MHz
Power	500mw	408mw	280mw	530mw

Timing Verification

- Late Arrival of Time cleaned SDF for verification.
- Simulating all timing critical paths with in tape-out schedule
  - Timing closure takes substantial time based on the complexity
- Longer run and debug times
- Is there a way to start Gate level timing simulations even before STA is complete??