Top Verification Challenges

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1. Verification Completion

- Increasingly difficult job:
  - Increasing design complexity
  - Shorter design cycles
  - "Hard – to – verify" designs
  - Specification issues
  - "Feature creep"
- Resource limitations
  - Dedicated verification leads
  - Design team conversant with HVL
- Proliferation of methods & tools
  - Formal, Dynamic, Assertions, Mutiple HVLs / Methodologies
  - Requires "all-round" team members

2. Reuse

- Reuse methodologies minimise the amount of coding
  - But, good design up-front to properly utilise reuse:
    - Module to Module (Horizontal)
    - Module to Chip (Vertical)
    - Project to Project (Horizontal)
- Ensuring reusability
  - Guidelines, linting?
- Verification IP
  - Selection of external VIP
  - Management and ownership of internal VIP
  - Quality control

3. Mixed Signal Verification

- Functional integration of analogue & digital
  - Late discovery of "simple" problems
- Paradigm shift for engineers
  - Ad-hoc analogue verification technique
  - Digital team consider analogue a "black art"
- Extending MDV to mixed-signal
  - Choice and fidelity of the analogue model:
    - SPICE, AMS, Real number modeling
  - Building a mixed-signal coverage model
  - Choosing appropriate constraints

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