Top Verification Challenges

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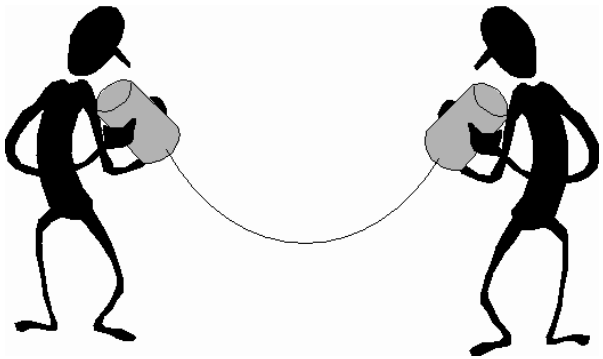
Communication vs Integrity



- **Challenge**: How can we guarantee the most fluent and accurate communication in a Chip?

- Example of **Interconnect** verification in SoC environment: How can we build the faster and most efficient verification environment for:
  - Data transfers integrity
  - Transaction integrity (Transaction shape are guaranteed through interconnects)
  - Memory mapping integrity (Physical addressing)
  - Performance integrity (Bandwidth and latencies calibration according to priorities)
  - Communication integrity (No deadlocks, protocol compliancy)

Genericity vs Coverage

- **Challenge**: How can verification catch-up with the challenge of ICs features and interfaces diversification ?

- Example: How can we cover all **functional muxing** of PADs for both implementation and specification checks ?

Development Phases vs Anticipation

"The early bird catches the worm"

OR

Early verification catches Bugs !!

- **Challenge**: How can verification anticipate very early issues emerging in next developments steps ?

- Examples:
  - Can RTL verification anticipates **final netlist** issues (X-propagation, low power issues, clock domain crossing issues …)
  - Inter-Chips verification, how can we manage parallel developments and verification in a **platform** ?