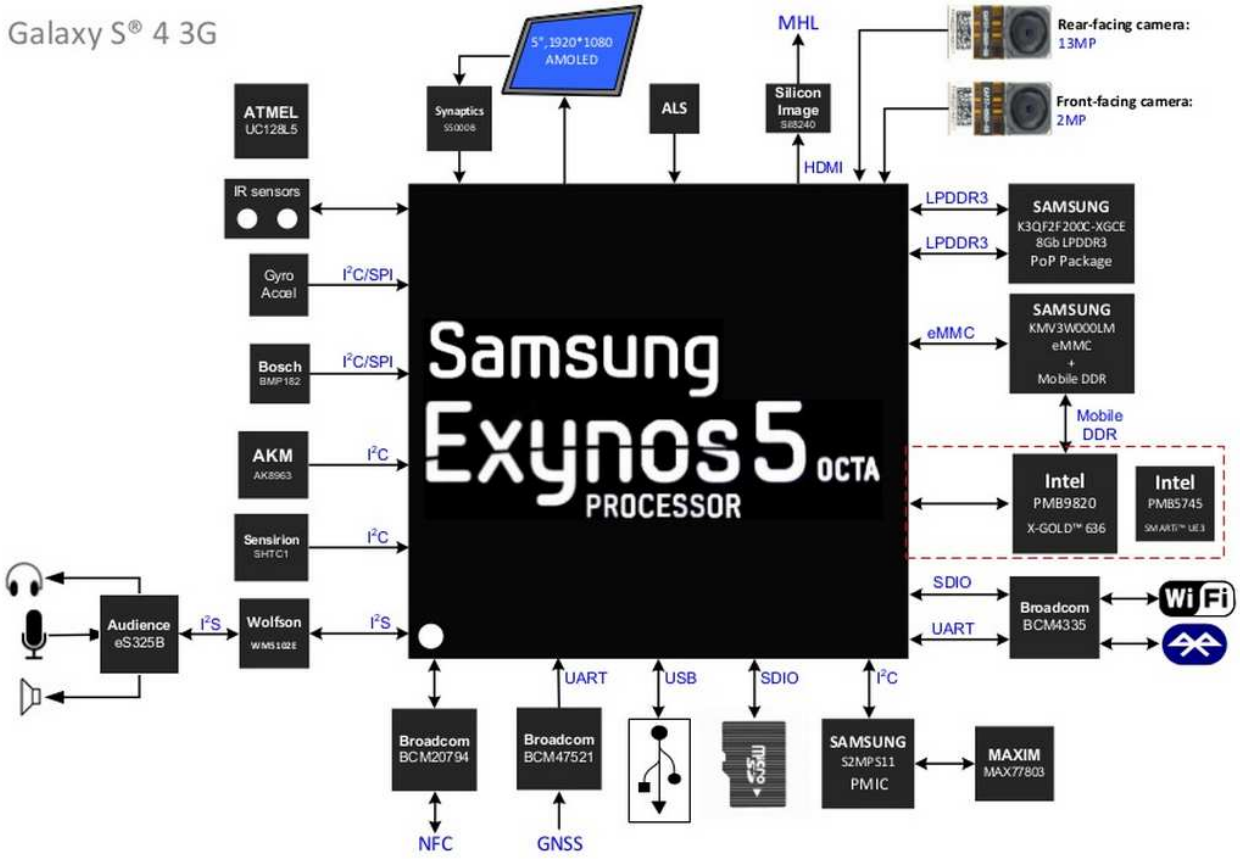
Verification futures 2013



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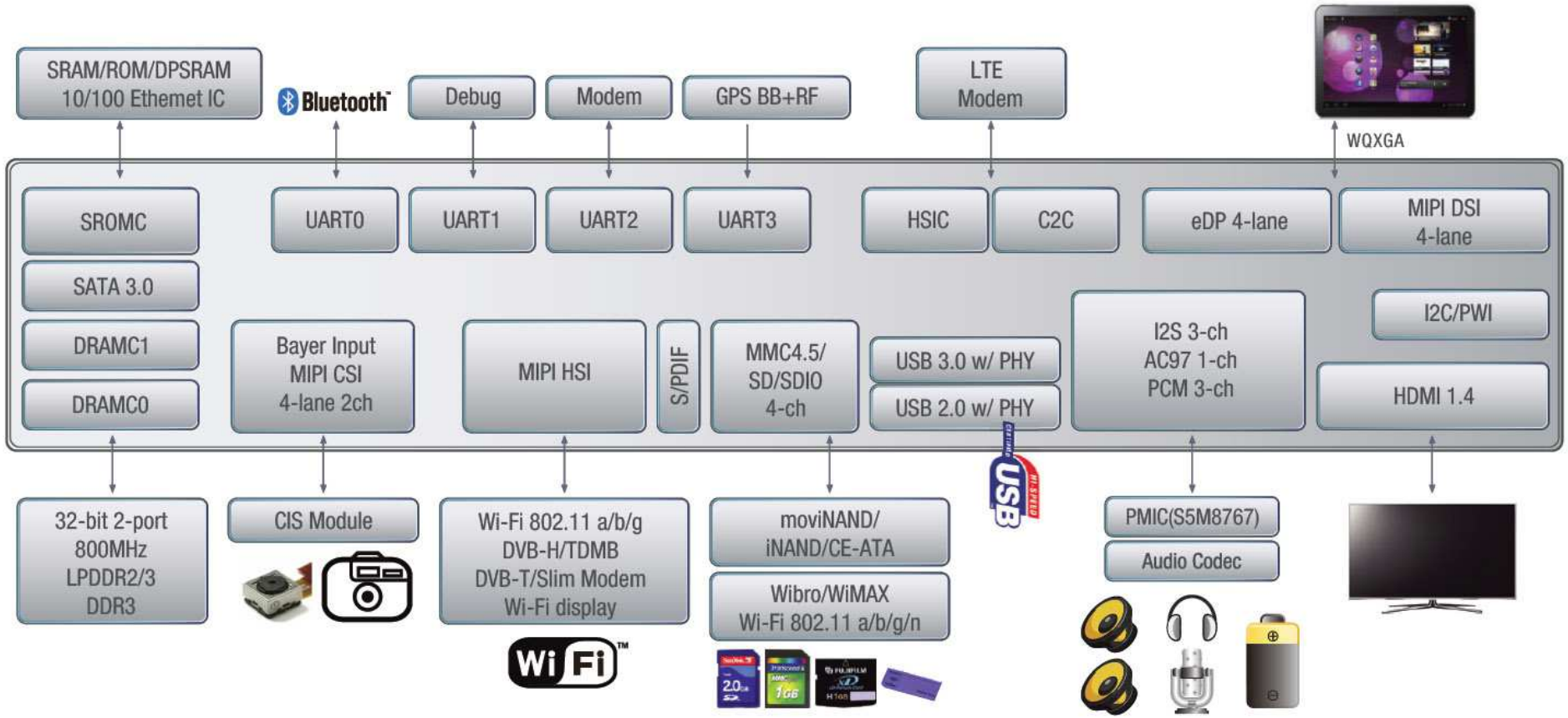
Context : SOC-IP verification



Introduction

Inte//gration :

Going from IP to SOC through Subsystems, quickly, safely and predictably…

Facts :

- **90%+ of modern ASIC SOCs logic area is reusable IP**
- **SOC-level verification can take 30%+ of the project's resources**
- **Most of the functional bugs found on silicon would be caught through a proper IP/SS/SOC verification partitioning**
- **IP deliveries from vendors are mostly integration or physical design-related, very few are verification-related**

Challenges

Our 3 challenges for IP vendors :

- **Sign-off integration verification plans**
- **Verification SW libraries**
- **Integration coverage toolboxes**

Sign-off integration verification

A sign-off list of features that needs to be verified in order to guarantee a correct integration of the IP

- **Necessary and sufficient**
- **Allows the SOC verification to focus on the integration, interfaces and interoperability**
- **Leaves the IP-specific functionality responsibility to the IP provider**
- **Saves time and resources**
- **Guarantees a perfect integration and interoperability**

Must include :

- **Clock, Reset, Bus interfaces, Specific functional interfaces…**
- **Functional, performance, power management, security requirements…**

Verification SW libraries

Aimed at SOC verification only

Written in real or pseudo code but executable format in any case :

IP registers description

- **Exhaustive description**

Programming sequences

- **Need to describe the minimal sequences to exercize the main IP functionalities**
- **Compact-enough to be simulation friendly**
- **Focusing on stressing the IP integration into the SOC**
  - **Functionality**
  - **Performance (BW, latencies…)**
  - **Power-management**
  - **Security**
  - **Any IP-specific aspect…**

Integration coverage toolboxes

- IP+VIP bundles
  - Ready-to-integrate packages
  - Removes the hassle to have to find, buy and match a VIP to each IP
  - In this context, VIP don’t have to be exhaustive as for IP-level verification, they must fit the integration verification objectives
- Scoreboards, callbacks…
- Assertions
  - Main industry-standard languages
  - Clock-gating, reset checks
  - Performance
  - Power-management
  - Security
  - Any IP-specific aspect…
- Sign-off IP-integration coverage report
  - Leveraging the above materials on the SOC-level simulation

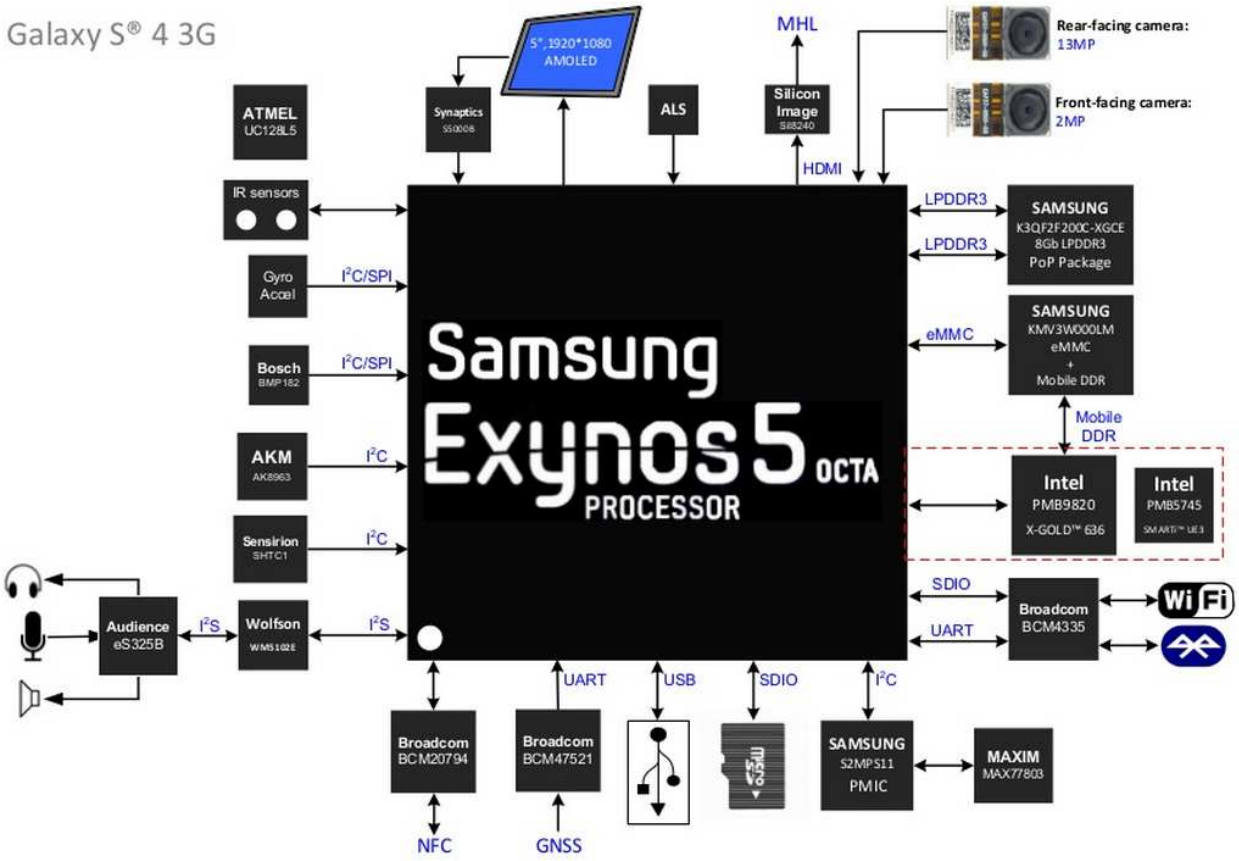
Conclusion

Verification-ready IP bundles would have a much favorable impact on SOC integration, quality and time-to-market

- **Avoids the SOC vs IP level verification dilemma**
  - **Each level sticks to well-identified, bound objectives**
- **Addresses the “Don’t know when to stop” syndrome**
- **Much of these materials should already exist at the IP level and could be adapted for such deliveries**
- **Reusable for subsystem-level verification as well**

- **Needs generalization**
- **Needs standardization**
- **Requires collaboration/alignment :**
  - **IP vendors**
  - **VIP providers**
  - **EDA tool vendors**

Thank you!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5",1920*1080 AMOLED
Synaptics S5000B
ALS
MHL
Silicon Image SiI8240
HDMI
Rear-facing camera: 13MP
Front-facing camera: 2MP
ATMEL UC128L5
IR sensors
Gyro Accel
I²C/SPI
Bosch BMP182
I²C/SPI
AKM AK8963
I²C
Sensirion SHTC1
I²C
Audience eS325B
I²S
Wolfson WM5102E
I²S
Samsung Exynos 5 OCTA PROCESSOR
LPDDR3
LPDDR3
SAMSUNG K3QF2F200C-XGCE 8Gb LPDDR3 PoP Package
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