Close Your Coverage Loop with Graph-Based Scenario Models

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SoC Verification Has a Problem

- The Universal Verification Methodology (UVM) is breaking down for full-SoC verification
  - Full-chip simulation too slow to run long random tests
  - No link between testbench and embedded processors
- Hard to hand-write C tests for embedded processors
  - Can't track multi-threaded, multi-processor tests in parallel
  - Hand written C-test are difficult to maintain and extend
- Weak quality metrics
  - Only interface toggle coverage
  - Hand written C tests == functional coverage

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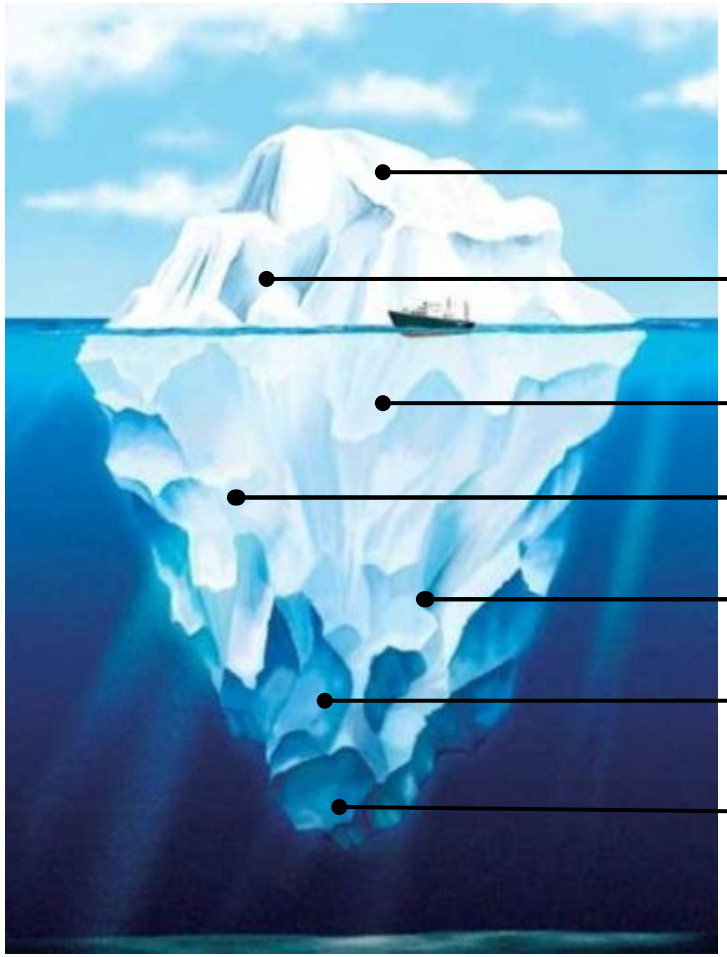
Today's Reality

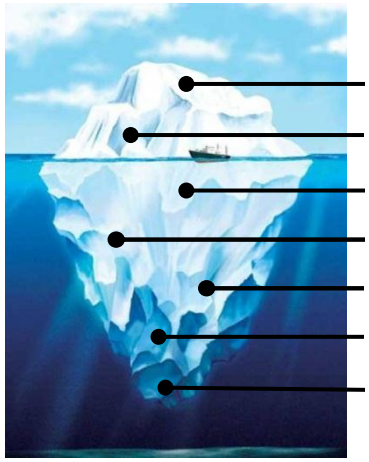
- Many SoC teams just "stitch and ship"
  - Run checks for connectivity of blocks within the full chip
  - Run a few sanity tests with an incomplete UVM testbench
  - Do basic IP integration testing with hand-written C tests
  - Insufficient coverage metrics at the full-SoC level
- Some SoC teams rely on emulation and prototyping
  - Bugs found post-simulation are harder to diagnose and fix
  - Bugs found late in the project tend to delay the schedule
  - Production software is well-behaved and unlikely to hit corner cases

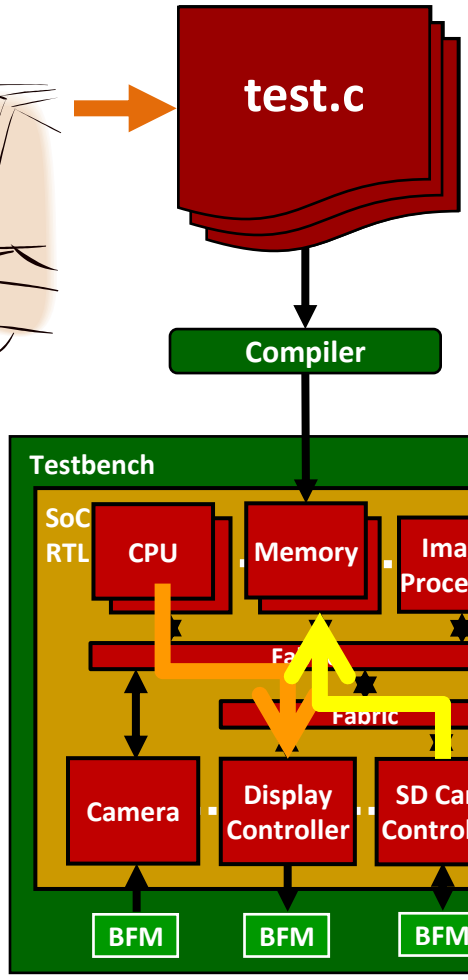
The SoC Verification "Iceberg"



- **Connectivity Tests**
- **IP Integration Tests**
- **System Use Cases**
- **Concurrency**
- **Coherency**
- **System and Power Management**
- **Performance Verification**

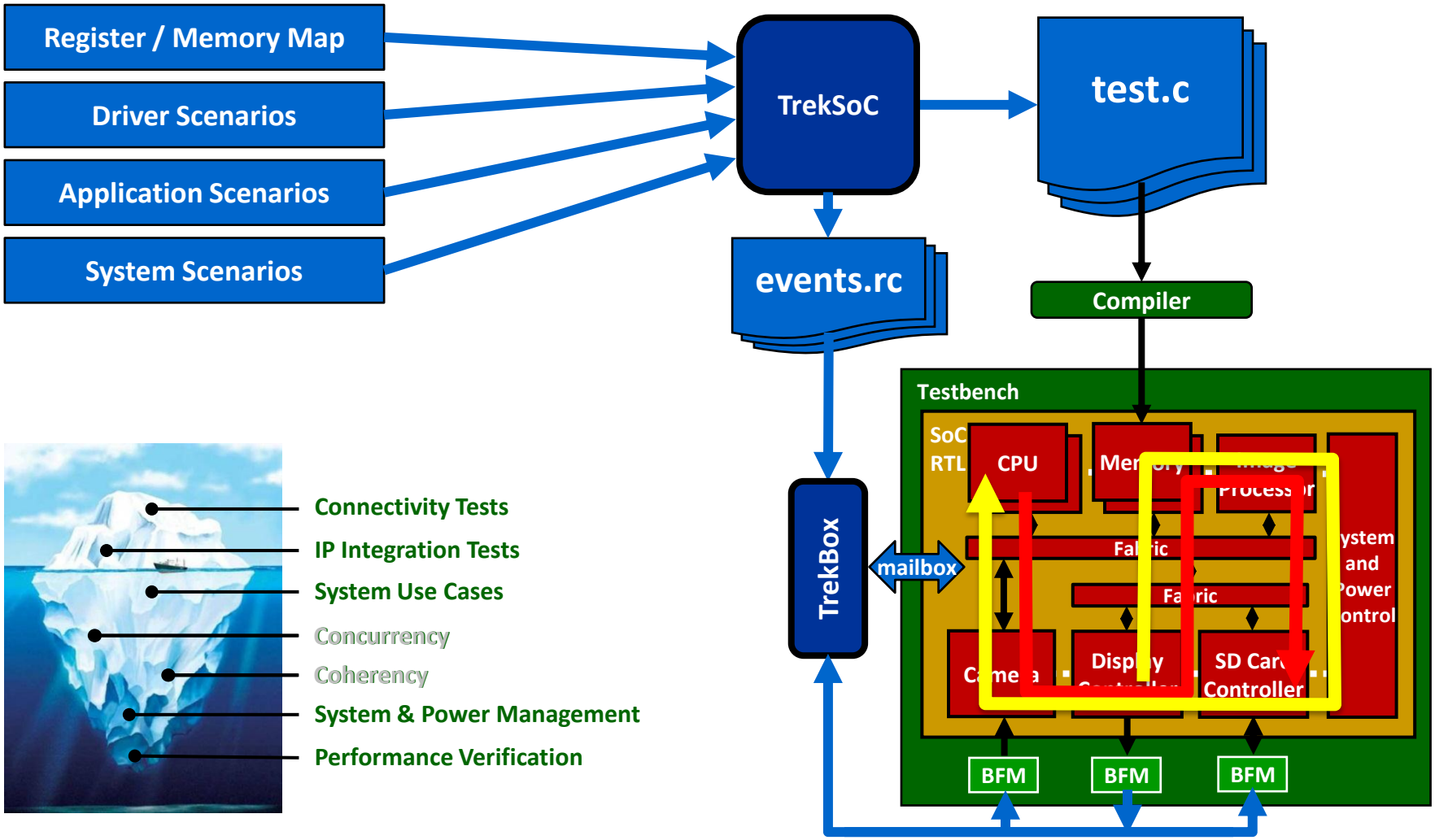
Manually Developed SoC Tests



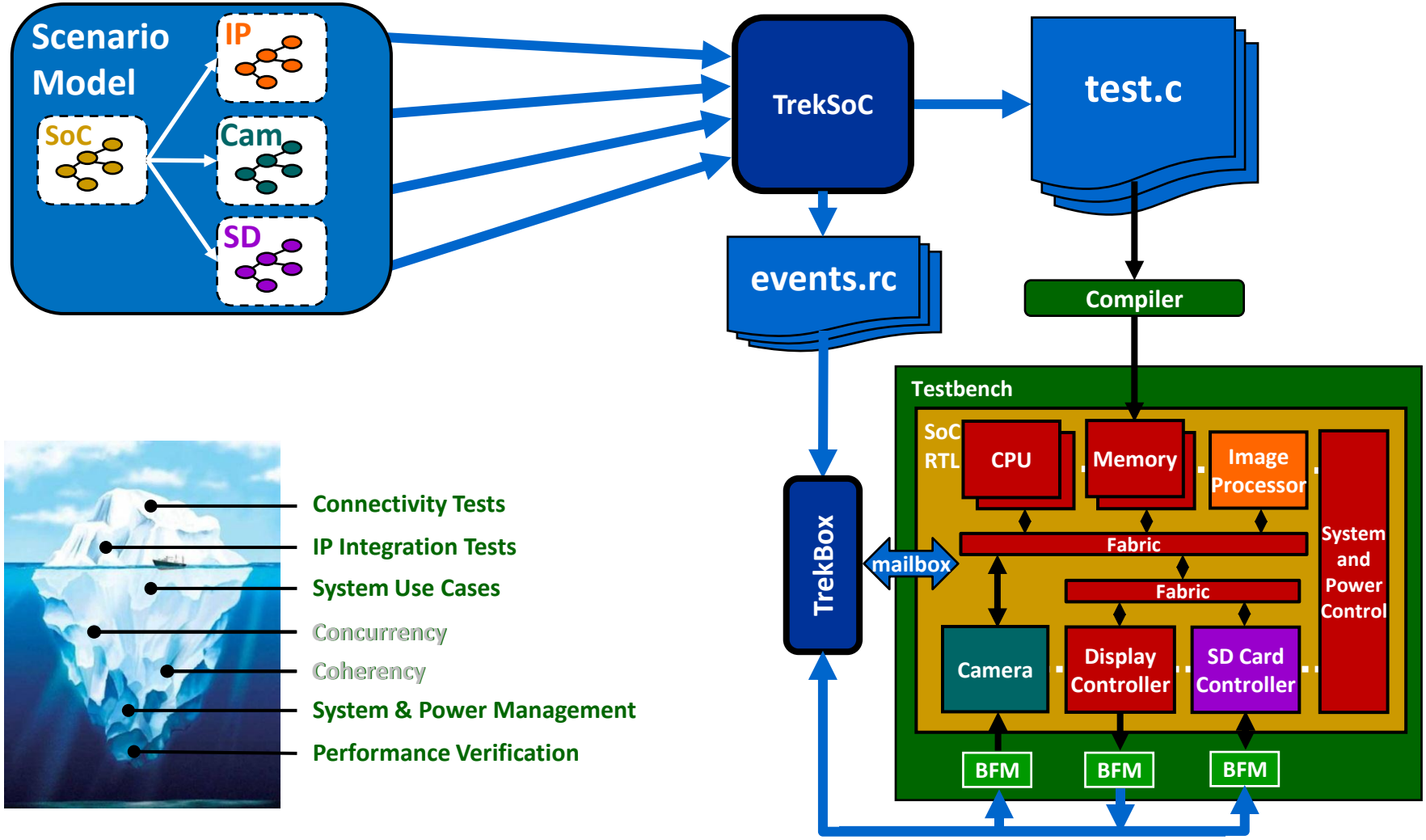


- Manual development and maintenance
- Difficult to manage:
  - Multiple threads
  - Multiple processors
  - Multiple memories
  - Interaction with I/O ports

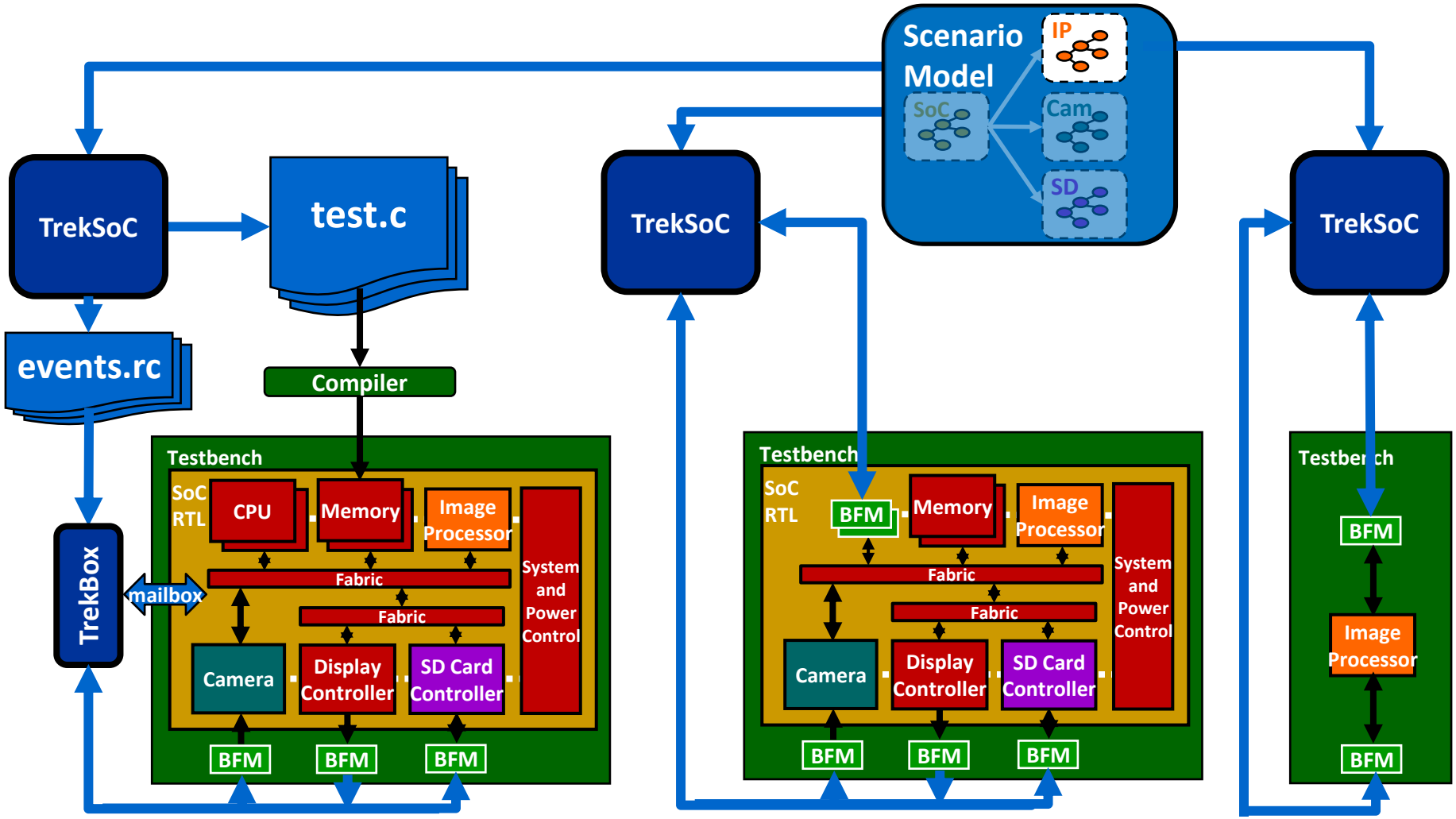
TrekSoC Automatic Self-Verifying C Test Cases



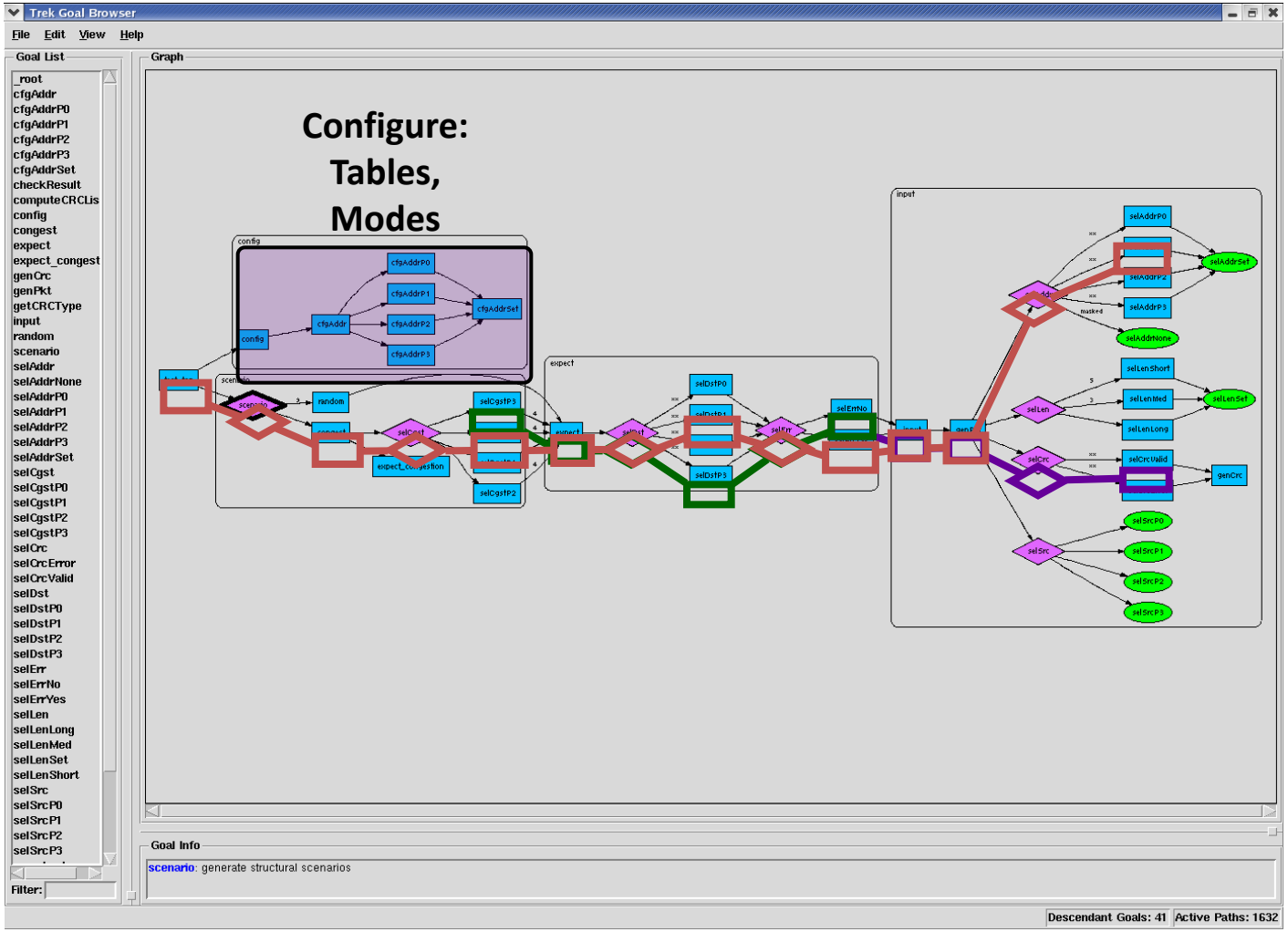
TrekSoC Automatic Self-Verifying C Test Cases



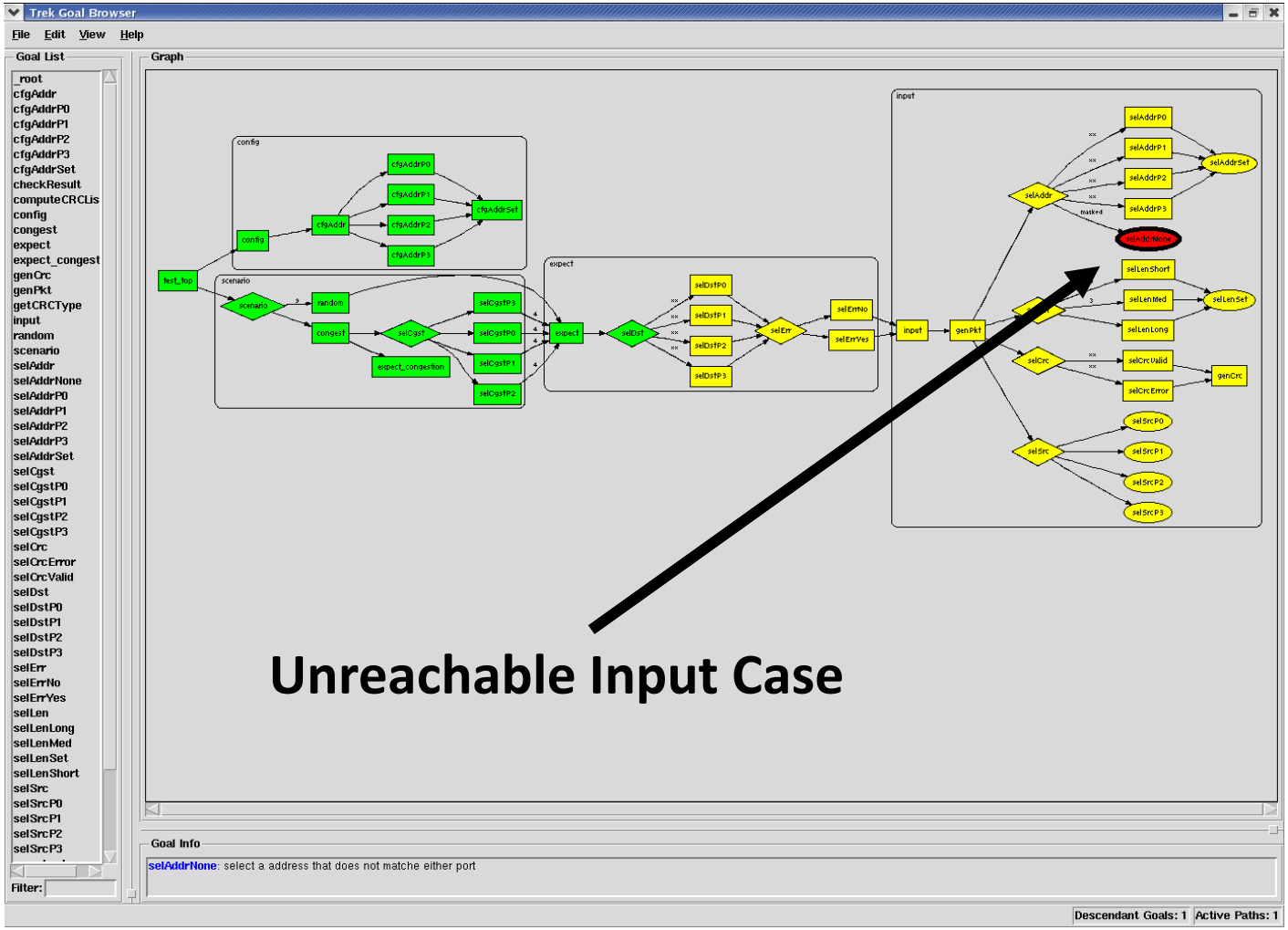
Multiple Design Level Support



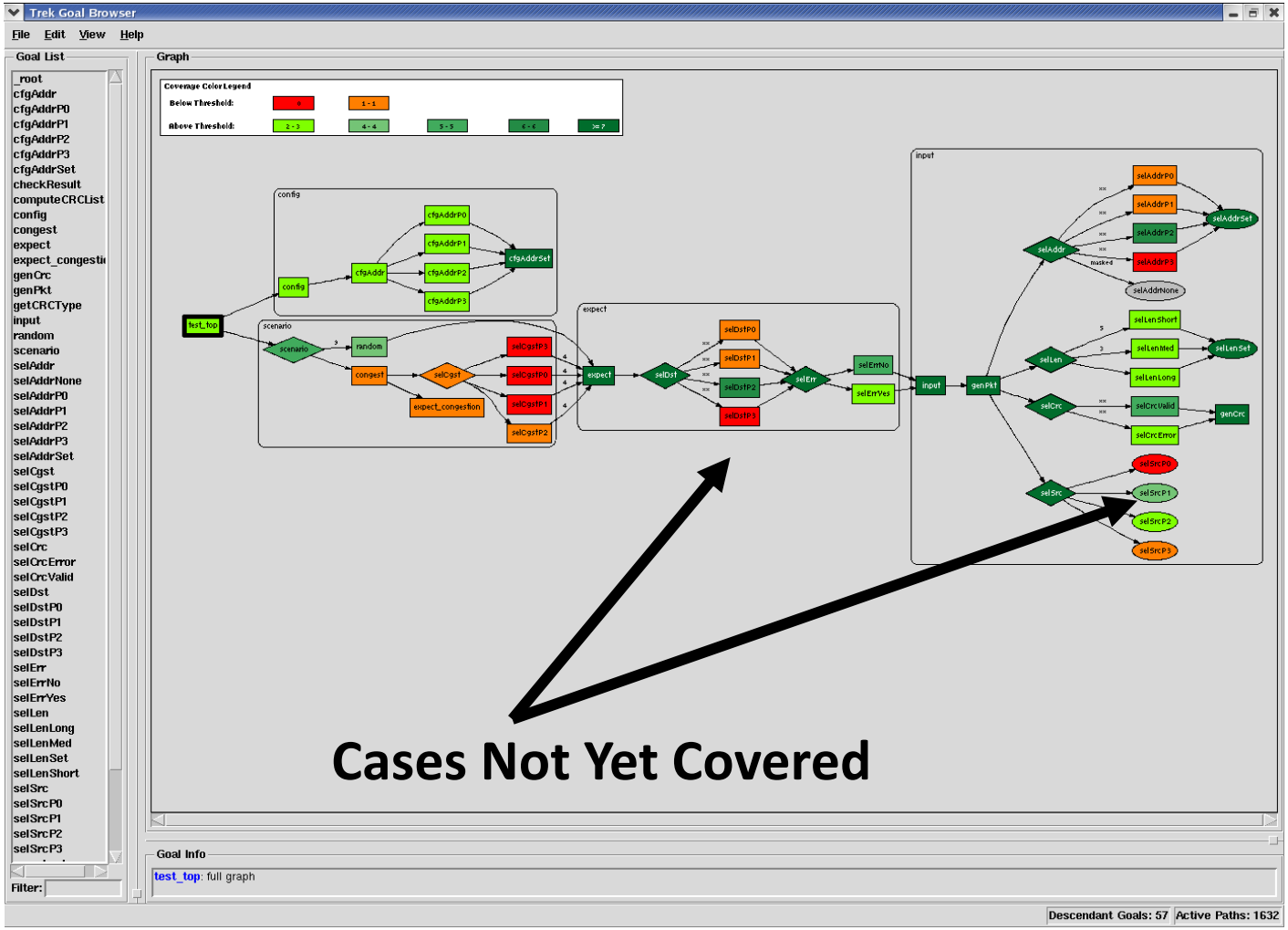
Scenario Models: Visualize Your Verification Space



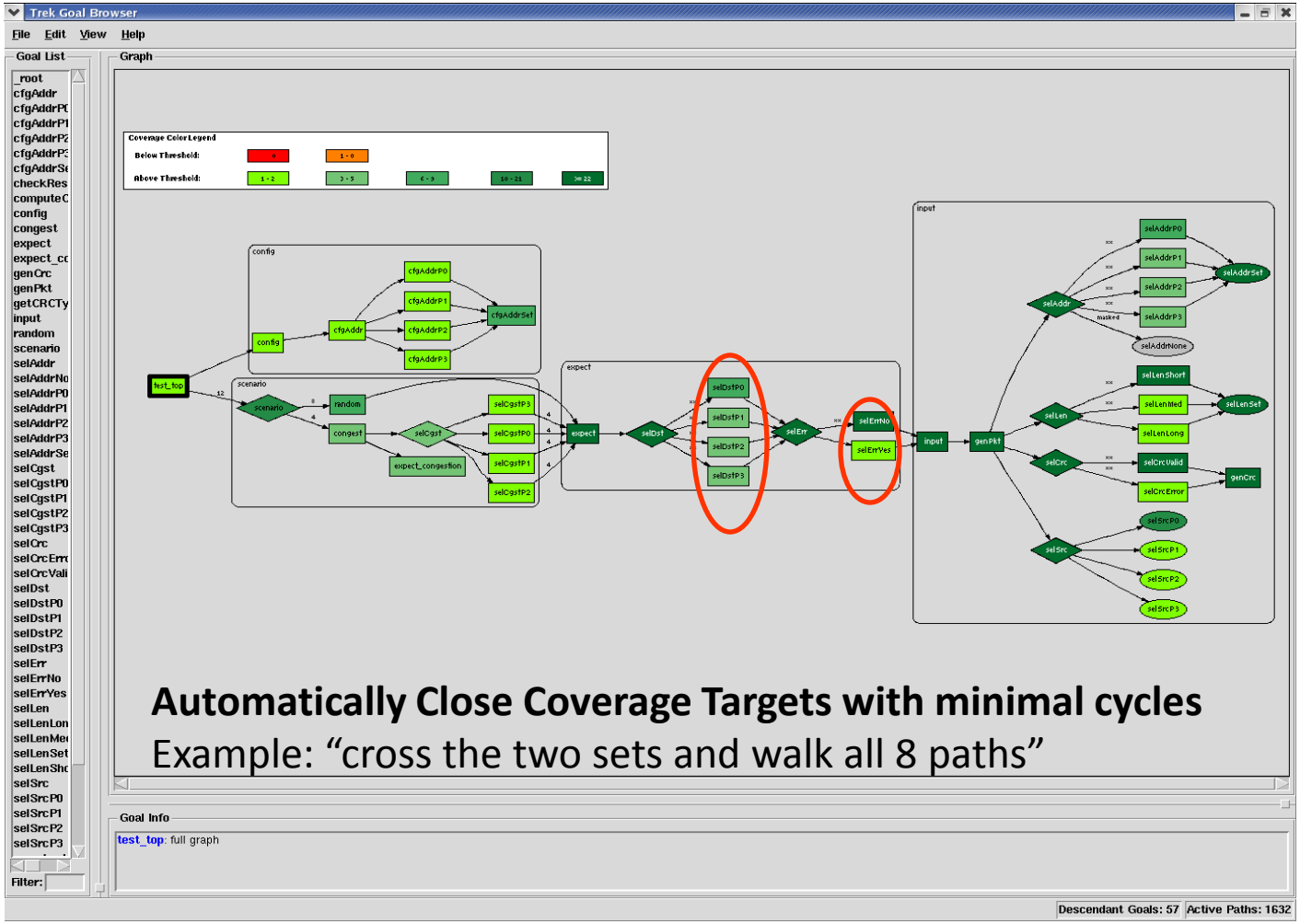
Pre-Simulation Reachability



Coverage



Closed-Loop Coverage



Automatically Close Coverage Targets with minimal cycles

Example: “cross the two sets and walk all 8 paths”

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Summary

- Stitch and ship verification is not sufficient for an SoC
- TrekSoC automatically generates C test cases
  - Run on the embedded processors and link to testbench
  - Quickly satisfy your functional coverage requierments
  - But still generating deep corner case scenarios
- Scenario models are easy and natural to create
  - Graphs efficiently capture verification knowledge
  - Graphs help internal communication and allow teams to define the functional coverage requirements

Thanks for Listening!