

Does ESL have a role in Verification ?

Nick Gatherer

Engineering Manager

Processor Division

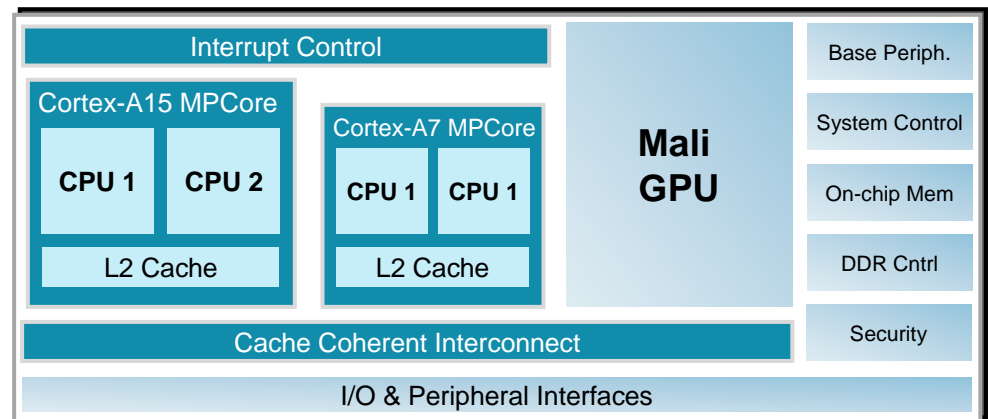
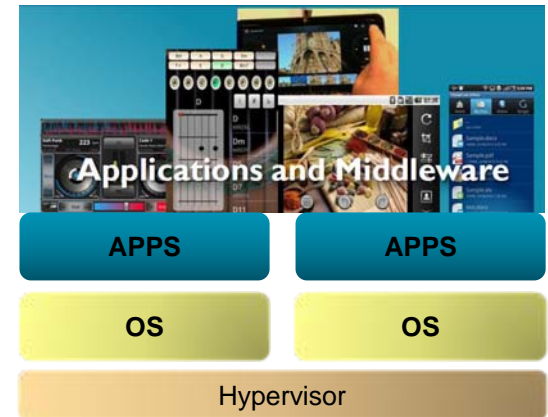
ARM



Key Trends

A typical verification challenge ...
big.LITTLE heterogeneous multicore

- Increasing complexity
- Increasing SW content
 - Multiple OSs
 - Secure services
- Higher performance, lower power
- Decreasing cost and time to market



Are we building the thing right ?

Are we building the right thing ?

Pillars of Verification Productivity

Contributors to Productivity Improvement

Tools & Methods

Tool perf, capacity,
& usability

Advanced Methods

Constrained random
ABV
Formal
Coverage

Verif. Platforms

RTL, FPGA,
Emulation

Re-Use

IP Re-use
Internal & 3rd party

vIP

Protocol checkers

Verification Stds

PSL/SVA
VMM/OVM/UVM

Protocol Stds

AMBA, MIPI, ...

Abstraction

Improved clarity
Minimal impl. detail

Efficient code

Fewer bugs

High Level

Lang. & Tools
C/C++/SystemC
Synthesis

Interoperability

Stds
UT, LT, AT, CA
TLM2.0

What is ESL ?

Electronic **System** Level

Behavior

Algorithms

Specification

HW / SW

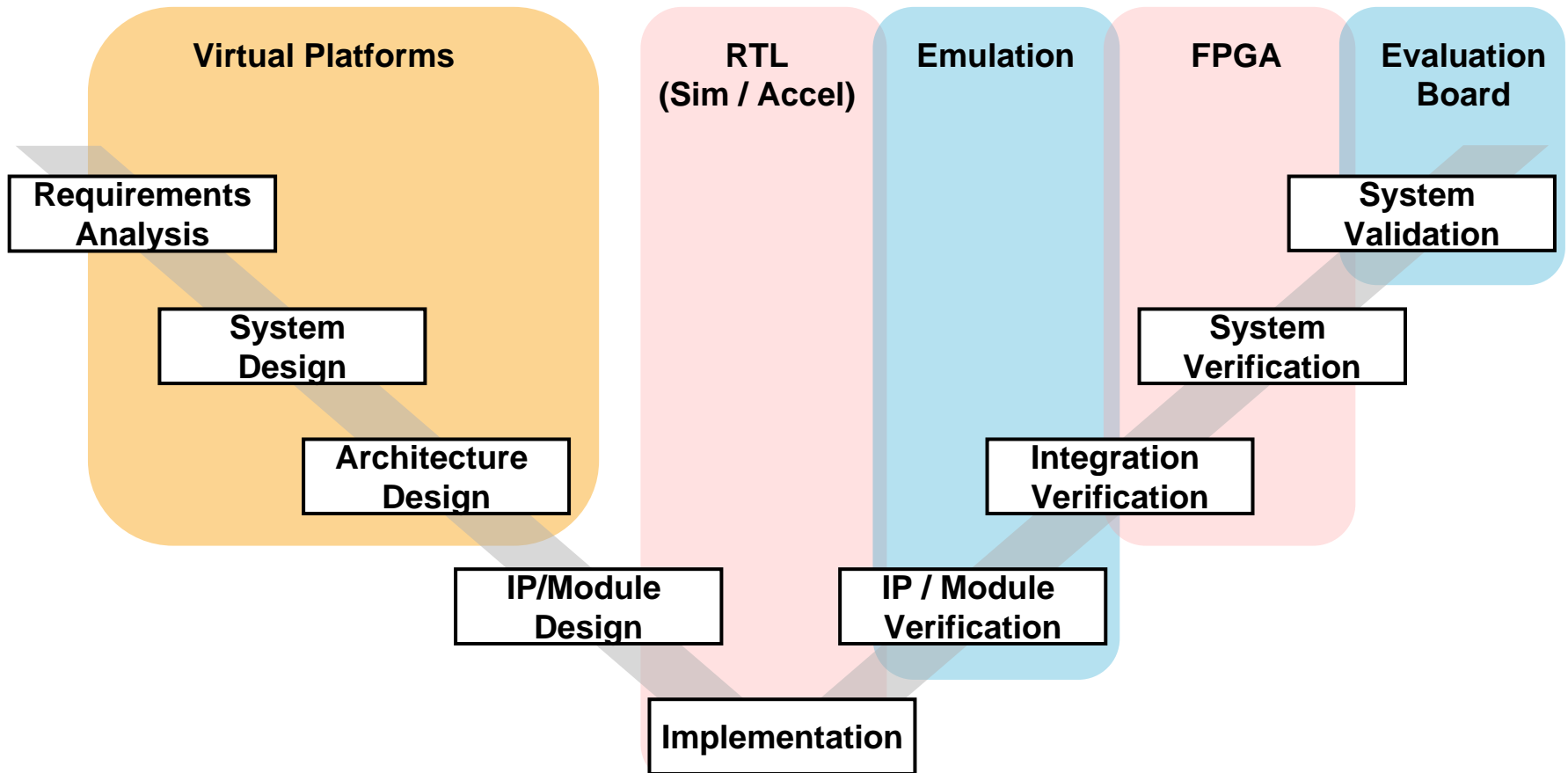
Architecture

Platforms

The ESL focus at ARM is on high level modeling to facilitate virtual platforms

SoC Verification Landscape

- Complex designs need multiple verification & validation platforms
- Virtual Platforms allow early HW / SW co-development & analysis

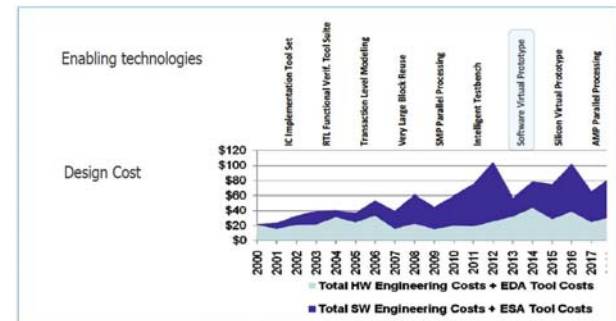


High Level Modeling at ARM

- ARM exploits high level modeling and virtual platforms to improve development productivity and reduce Time to Market.
- Models are provided early in product development lifecycles
- Models are utilized for:
 - Architecture & device modeling
 - Early software development
 - Early HW / SW co-validation
 - Device implementation compliance
 - Device validation support
- Models are used ...
 - Within ARM
 - Supplied to silicon partners
 - Supplied to Ecosystem partners

Accelerating SoC Time to Market ...

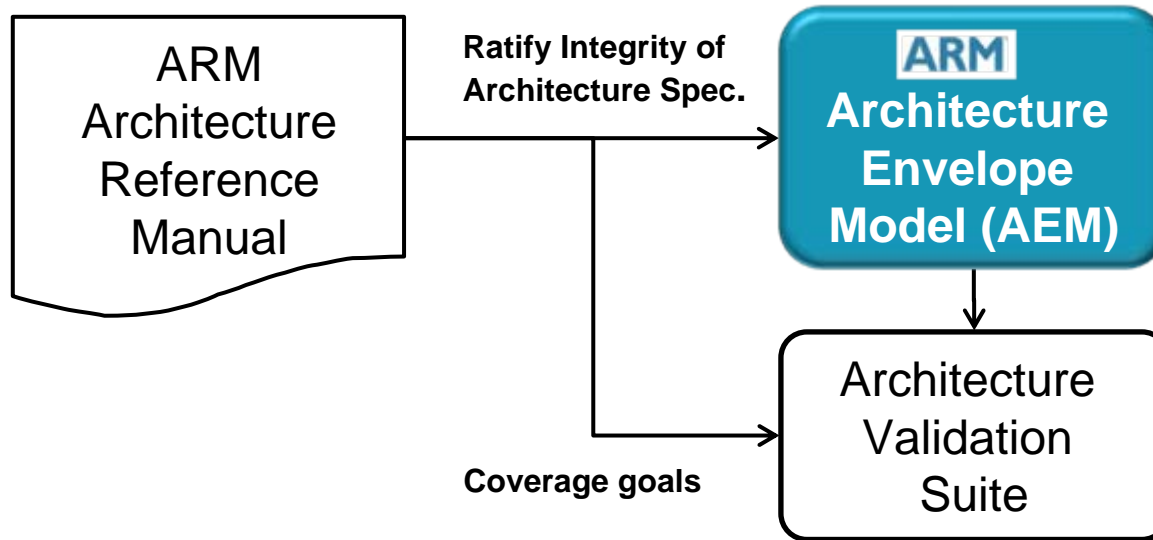
- High performance models suitable for SW community
- Available early for SW development
 - Accurate to HW for consistency
 - Easy to debug enabling improved productivity
- Easy to deploy to facilitate the developer community



Source: INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS: 2010 update

Architecture Modeling

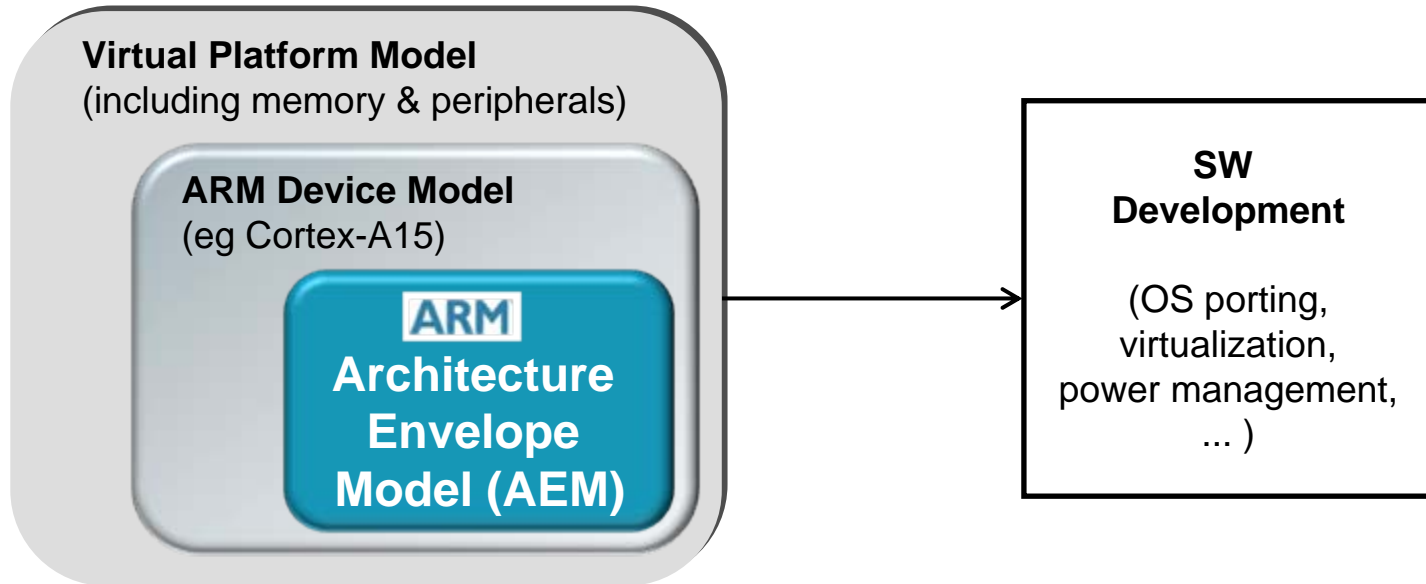
- The Architecture Envelope Model (AEM) is an executable version of the ARM Architecture Reference Manual



- Catch architectural defects early
- Optimal abstraction level for debug; Fix bugs early at minimal cost/time
- Ensure consistency of Architecture spec, AEM, and validation suite

Early HW / SW co-validation

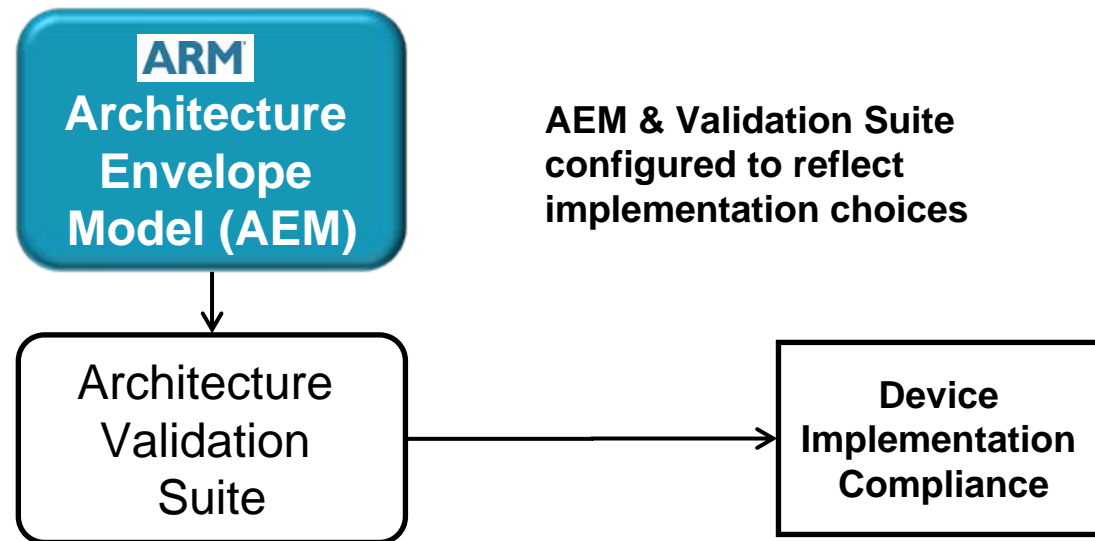
- Models are used as an early software development platform



- Early validation and debug of HW / SW interaction
- Opportunity to fix architecture before committing to implementation
- Provides platform to support Ecosystem development

Device Implementation Compliance

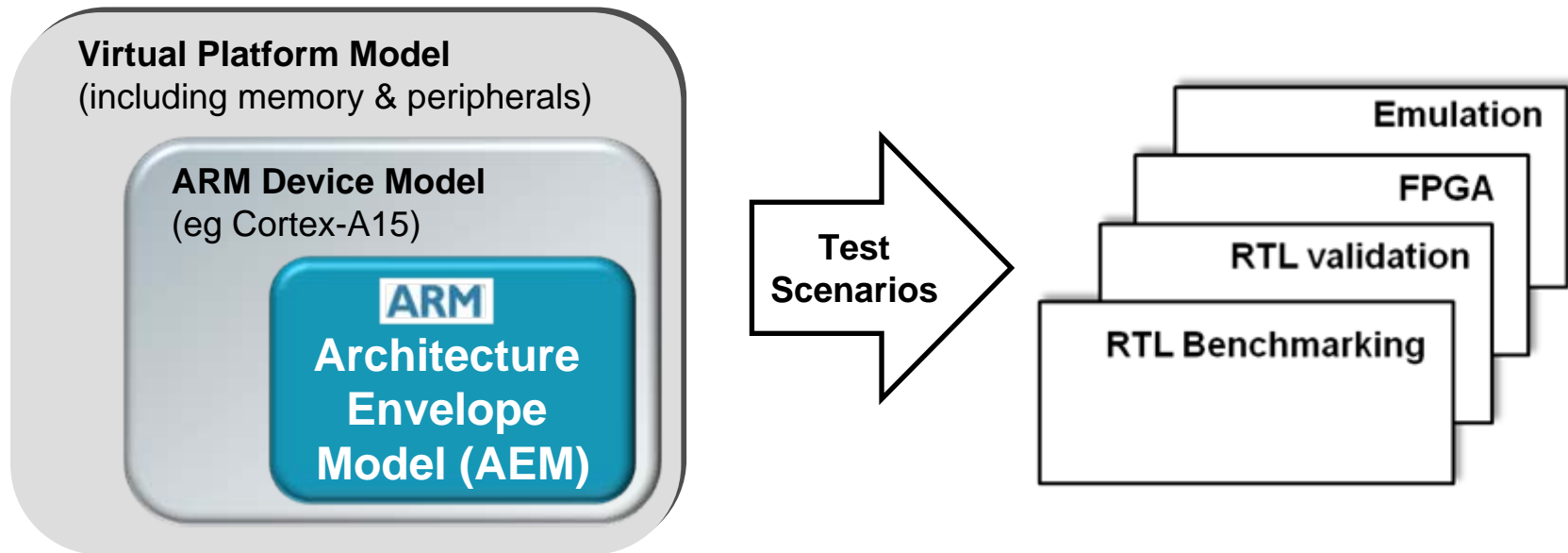
- The AEM is used as a definitive architecture reference



- Evaluate architecture compliance of HW device implementations
- Protect validity & value of the ARM Ecosystem

Device Validation Support

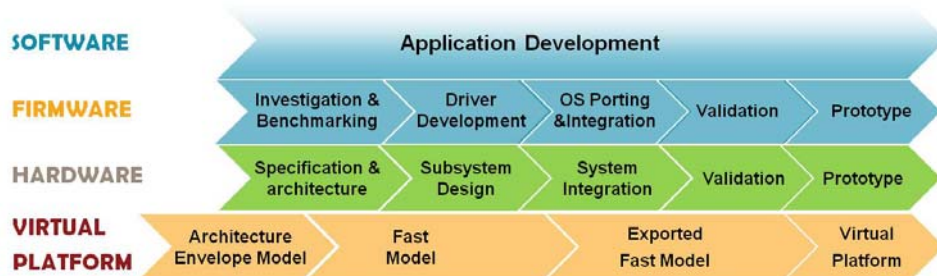
- Models are used to develop SW-driven test scenarios



- Develop test scenarios before executing on target
- Known-good test scenarios ready when validation platform available
- Separate concerns; Improved debug effectiveness & productivity

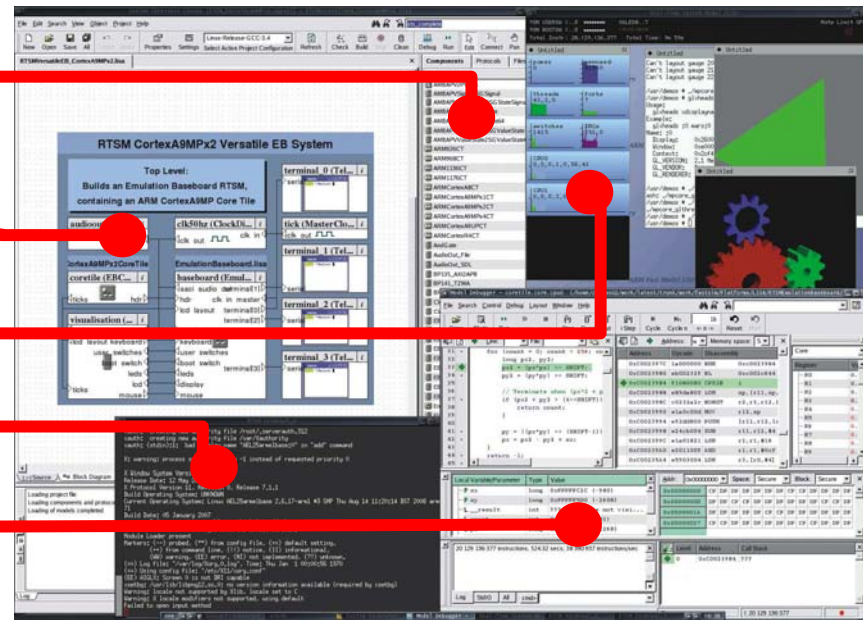
ARM Fast Models

- Comprehensive model portfolio of ARM CPUs, peripherals, and complex system IP
- Models available early, even for new ARM architectures and IP
- Programmers view abstraction level
- High simulation speed (up to ~ 200 MIPS)
 - Suitable for software development
- Comprehensive debug support including ARM DS-5
- All models validated and supported by ARM
- Export to a wide range of ESL environments (SystemC/TLM2.0)
 - Enables ARM partners to create comprehensive Virtual Platforms through 3rd party EDA solutions
- Models configurable to support a range of development tasks



ARM Fast Models

- Rich model portfolio (CPUs, periph, system IP)
- Configuration canvas
- Visualization
- OS console & status
- Extensive debug & trace



Common Tool Chain – ARM DS-5



Fast Model



Development



Final Product

ESL Future Challenges

- Model availability & Ease of Use
 - To maximize added value, models need to be available early and with validated quality
 - Need to empower new ESL users through the provision of comprehensive platform models
 - Can formal techniques be applied more broadly to validate equivalence between ESL and implementation abstraction levels ?
- Scalability
 - Need to improve simulation performance for increasingly complex platforms
 - multicore ... manycore ... complex system solutions
- Standardization
 - Need to avoid proliferation of modeling abstraction levels
 - Need standardization for the characterization and instrumentation of performance and power modeling

Conclusions

- ESL can be used effectively to complement implementation focused verification & validation platforms
- ESL is particularly compelling in the domain of systems and architectures, and offers unique value in the early phases of product development.
- ARM exploits high level modeling to improve productivity and reduce Time to Market, and as part of a holistic verification & validation strategy
- Within the verification context, models are used to ...
 - Confirm integrity of architecture specifications
 - Facilitate early HW / SW co-validation and debug
 - Evaluate architecture compliance of device implementations
 - Development and debug complex test scenarios for device validation
- ARM delivers and supports high level models through the ARM Fast Models product

For more information www.arm.com