

Multi-Core Architecture for Networking

Bill Lynch

www.huawei.com



Summary

It's about the same.

Except where it's different

- a lot of cores (32-256)
- special accelerators
- datapath sometimes separate from header path with its own accelerators

Problem to be solved

- **Allocate buffers and get the packet into memory**
- **Parse the destination out of the packet**
- **Lookup a potentially large and complicated destination table**
- **Datapath processing (crypto, dpi, compeess, ...)**
- **Queue up the packet to egress to correct destination**
- **Schedule the egress from amongst available packets (often with complicated parameters)**
- **Do some accounting/billing/resource management**

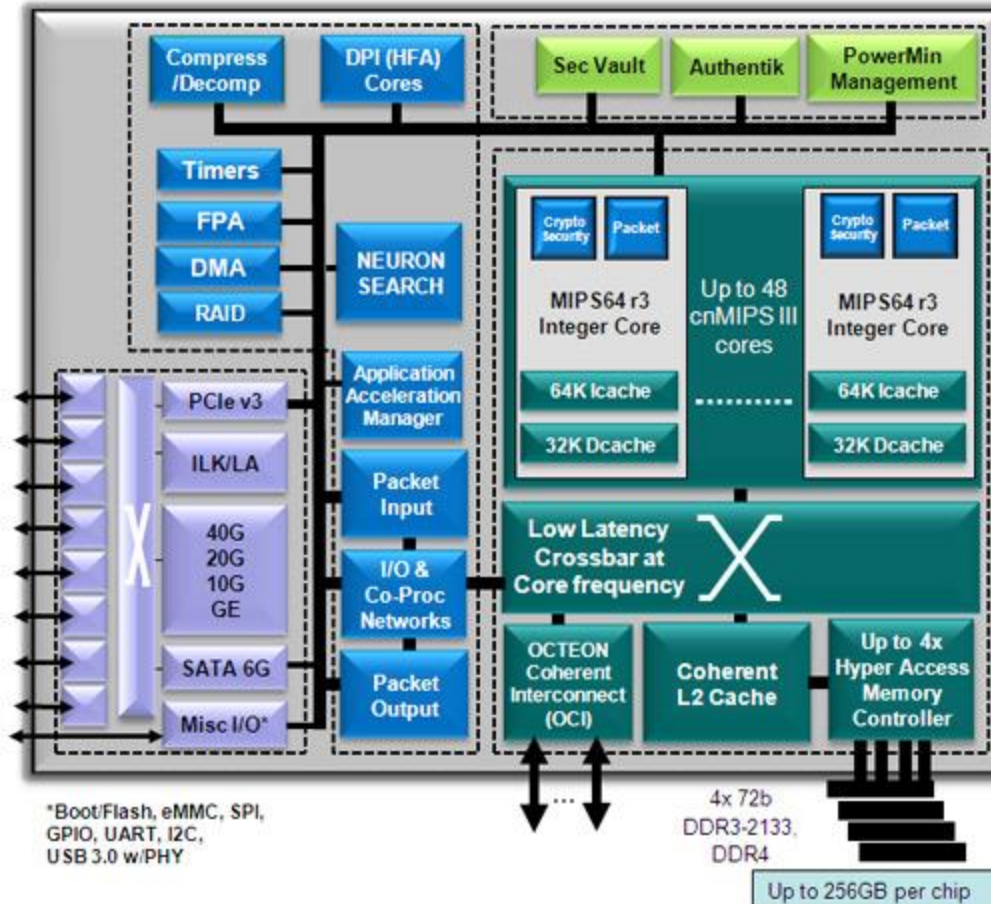
Overview/Trends

- **Packet processing services with easier programming model**
 - Protocol processing (IPv4, IPv6, MPLS, QinQ, IP Multicast etc.)
 - Table lookups
 - Traffic Management/Engineering
 - Header Encapsulation/De-encapsulation/Modification
- **Datapath processing**
 - Crypto
 - (de)compression
 - Dpi
- **Multi-core for higher throughput**
- **Most use RISC CPU implementations**
 - MIPS, ARM, ARC, Custom
- **NoC for connectivity**
- **Power is limiting factor**

Programming model

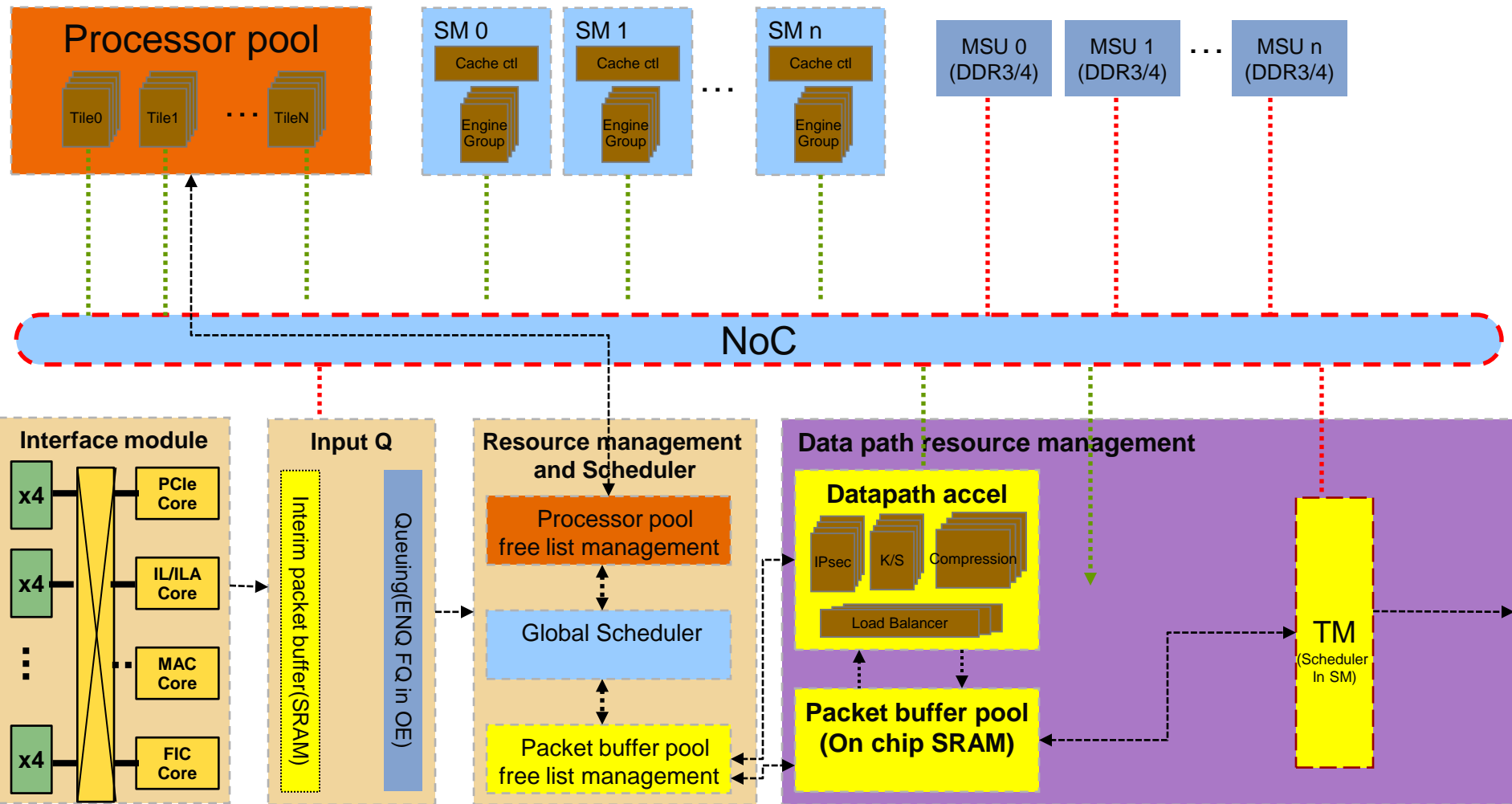
- **Evenly split between run-to-completion and software pipelined**
- **Cache coherence becoming universal; used to be uncommon**
- **Most can now run an OS; used to be uncommon**
- **High-end multi-core processor usually support throughput in the range of 80Gbps to 200+Gbps**
 - Requires careful management to avoid cache thrashing
 - Memory BW required about 6x throughput

Cavium Octeon Processor



Source: http://www.cavium.com/OCTEON-III_CN7XXX.html

Huawei Services Network Processor



Summary

- **Many cores: 32-256**
- **NoC, OS, coherence now common**
- **Accelerators:**
 - Datapath (crypto, (de)compress, dpi, buffer management, queueing)
 - Lookup (parsing, lookup, accounting)

Thank You

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