Multicore and MIPS: Creating the next generation of SoCs

Jim Whittaker
EVP MIPS Business Unit
Many new opportunities

- Wearables
- Home wireless for everything
- Automation & Robotics
- ADAS and intelligent transport
- IoT/IoE
  - Health
  - Energy
  - Agriculture
- Big data & analytics

Flexible CPU & heterogeneous processing key to catch the next wave
Imagination’s IP portfolio

Everything needed to create connected SoC solutions

FlowCloud
Connectivity

Ensigma
Communications Processors

PowerVR
Graphics & GPU Compute Processors

MIPS
General Processors

PowerVR
Video & Vision Processors

Unified Memory

Each IP core is a class leader - when used with any other processors
Lowest power - Smallest silicon area
Open and customer - centric business model
Why Multicore

- Number of transistors on a chip far exceeds the number we can use to increase single thread performance
- Methods used to increase single thread performance result in reduced power efficiency
- Workload dictates the optimum balance of compute resources
- Optimised hardware for specific tasks improve performance/power
Momentum - MIPS CPUs

Already deployed across the spectrum

32-bit embedded microcontrollers

64-bit advanced networking processors

...and everything in-between!
MIPS is strong – and growing

- Delivering the architecture
- Delivering the IP cores
- Building up the ecosystem
- Revolutionising security

Delivering the most compelling alternative for 64/32bit CPU IP

- >5B MIPS CPUs shipped
- Up to 40% smaller than competitors
- Industry’s leading CoreMark performance
- 64bit CPU IP shipping in volume for 20 years
And now...the next phase begins

I6400: not just the next MIPS CPU core – the next era of CPU IP
I6400: Broad feature set for a wide range of applications

- **Automotive/Embedded**: SMT, Virtualization, SIMD, Heterogeneous MC, ECC
- **DTV/STB**: SMT, Virtualization, SIMD, MC
- **Mobile**: 64-bit, SMT, Virtualization, SIMD, Heterogeneous MC
- **Enterprise**: 64-bit, SMT, MC, Multi-Cluster, Virtualization, ECC

*Brodest set of applications ever addressed by a single MIPS core family*
I6400 – A MIPS64 AND MIPS32 processor

- **MIPS64**
  - Is MIPS32, plus instructions for 64-bit data types
  - Runs MIPS32 software without mode switching

- **MIPS64/32 Release 6**
  - Streamlining a highly efficient architecture
  - Modernization of architecture through:
    - Additional instructions for enhanced execution on modern software workloads =
    - JITs, VMs, PIC, etc. commonly found in Javascript, Browsers, abstracted compiler technologies (i.e. LLVM)

**MIPS: the ultimate 64/32-bit architecture**
I6400 Multi-threading

A powerful differentiator among IP cores

- Why MT?
  - A path to higher performance, and higher efficiency
  - 30%-50% higher performance for 10% increase in cluster area*
    - Ex. CoreMark, DMIPS, SPECint2000
  - Decades of multi-threading expertise in MIPS and Imagination

- Easy to use – programming model is same as multi-core
  - A thread looks like a core to standard SMP OSs

- Simultaneous multi-threading (SMT) execution
  - Multiple threads execute in a given pipeline stage per cycle, or…
  - Superscalar execution on a single thread
  - Thread execution can switch dynamically per cycle

* Preliminary performance benefit on popular benchmarks for adding a 2nd thread in I6400 processor, with silicon area cost
MIPS64 I6400 - hardware virtualization highlights

Rich set of Trusted Execution Environment features and benefits

- **Secure**
  - Root is the secure hypervisor/kernel
  - Guest access rights controlled by Root
  - Full VZ using Root/Guest TLB

- **Scalable**
  - Supports up to 15 Guests (OS and/or Apps)
  - SoC virtualization support
    - Virtualized GIC (interrupt controller) and IOMMU
    - Bus transactions to other IP include Guest ID

- **Benefits**
  - Ease of use - no modification required to Guest OS
  - Reliability – corrupted/crashed OS1 cannot affect OS2
  - Performance – intelligent resource allocation
  - Security – multi-domain support in hardware
MIPS64 I6400 base core microarchitecture

Optimized for efficiency and maximizing pipeline utilization

- Dual-issue In-Order design with MT
- Compact, balanced 9-stage pipeline
- Dual issue 128b SIMD (Int, SP/DP FPU)
  - IEEE 754-2008 compliant FPU
- Instruction bonding on integer, FP ops
  - Doubles throughput on memcopies
- Instruction and Data L1 caches w/ ECC
  - 64 byte cache lines
- Advanced Branch Prediction
- Low latency 128b core:CM interface
MIPS64 I6400 multi-core features

Leverages new coherency architecture

- Coherent cluster, up to 6 cores
- Directory-based coherency improves power, performance and scalability
- PowerGearing for MIPS
- Virtualized GIC and IOMMUs
- Integrated L2 Cache (L2$)
  - 512KB – 8MB (16-way) with ECC
  - Low L2$ hit latencies
  - HW prefetch lowers latency to memory
- AXI4 -> ACE System Interface
  - Multi-cluster, heterogeneous scalability
Building systems:— Threads, cores and clusters…

1 Thread Core  2-4 Thread Core  2-6 Core Cluster  2-64 Cluster Node
Building systems:- Threads, cores and clusters…

1 Thread Core

- Wide range of CPU configurations
- Hardware virtualization based security
- PowerGearing™ power management

2-4 Thread Core

2-6 Core Cluster

2-64 Cluster Node

SoC Fabric
Flexible configuration for flexible needs

- **Hardware multi-threading**
  - 30%-50% more performance for 10% more area

- **Multi-core**
  - Mix of cores/configurations

- **Multi-cluster**
  - Mix of heterogeneous CPU clusters

Embedded

Consumer/STB

Mobile

Server

Storage

Dataplane
It’s not just CPUs – true heterogeneous processing

Single Thread  Multi-Threaded Core

Multi-Core CPU Cluster  Multi-Core GPU Cluster
IP Platforms: Heterogeneous Network Processors

MIPS leads the way in security, hardware multi-threading, coherency – and efficiency

- Ensigma NPU
  - 10/40/100Gbps Offload
- PowerVR Multicore GPU Compute
- MIPS Coherent Multicore Cluster
- Coherency across thread, core, cluster
- Terabit Coherent Fabric
- Unified Memory

Up to 40% better processor area for multi-core

Comprehensive support for hardware multi-threading

Customer Differentiating System IP
IP Platforms: Heterogeneous IoT Device Processors

High end feature set for deeply embedded = scales perfectly from high end

- **Ensigma**
  - RPU
  - BT Smart
  - Low Power Wi-Fi

- **Customer**
  - Differentiating System IP

- **MIPS**
  - M-Class MCU

- **SoC Fabric**
  - On-chip Flash
  - On-chip RAM

**Hardware Virtualization**
Tightly integrated, low power communications
Class-leading single thread performance
Conclusions

- Multicore is not just about multiple cores
  - Threads, cores and clusters – and not just CPUs

- The application space is getting wider
  - Flexible cluster configuration for power management and burst performance needs many options

- MIPS Series6 Warrior cores deliver a compelling alternative for multi thread/core/cluster CPU IP
  - Not just for CPUs, but for heterogeneous SoCs
Multicore and MIPS: Creating the next generation of SoCs

Jim Whittaker  
EVP MIPS Business Unit